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Evaluating the AD9550 Integer-N Clock Translator

FEATURES

- Converts preset standard input frequencies to standard output frequencies
- Input frequencies from 8 kHz to 200 MHz
- Output frequencies up to 810 MHz LVPECL and LVDS (200 MHz CMOS)
- Preset pin-programmable frequency translation ratios
- On-chip VCO
- Single-ended CMOS reference input
- 2 output clocks (independently programmable as LVDS, LVPECL, or CMOS)
- Single supply (3.3 V)
- Very low power: <450 mW (under most conditions)
- Small package size: 5 mm × 5 mm
- Exceeds Telcordia GR-253-CORE jitter generation, transfer and tolerance specifications

APPLICATIONS

- Cost effective replacement of high frequency VCXO, OCXO, and SAW resonators
- Flexible frequency translation for wireline applications such as Ethernet, T1/E1, SONET/SDH, GPON, xDSL
- Wireless infrastructure
- Test and measurement (including handheld devices)

GENERAL DESCRIPTION

This user guide describes the hardware of the AD9550 evaluation board. The AD9550 evaluation board is a compact, easy-to-use platform for evaluating all features of the AD9550 integer-N clock translator.

The AD9550 is a phase-locked loop (PLL) based clock translator designed to address the needs of wireline communication and base station applications. The device employs an integer-N PLL to accommodate the applicable frequency translation requirements. It accepts a single-ended input reference signal at the REF input.

The AD9550 is pin programmable, providing a matrix of standard input/output frequency translations from a list of 15 possible input frequencies to a list of 52 possible output frequency pairs (OUT1 and OUT2).

The AD9550 output is compatible with LVPECL, LVDS, or single-ended CMOS logic levels, although the AD9550 is implemented in a strictly CMOS process.

The AD9550 operates over the extended industrial temperature range of −40°C to +85°C.

DIGITAL PICTURE OF THE AD9550 EVALUATION BOARD

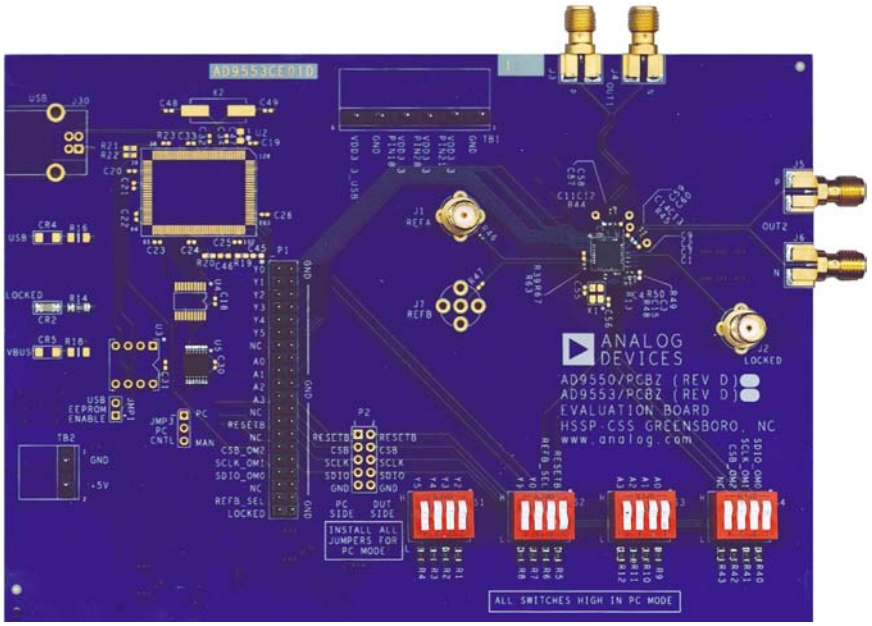

Figure 1. AD9550 Evaluation Board

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REVISION HISTORY

11/10—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The following instructions are for setting up the physical connections to the AD9550 evaluation board.

SETTING UP THE POWER CONNECTIONS

Set up the power connections as follows:

1. The AD9550 evaluation board is powered via the TB1 connector located in the top center of the evaluation board. Connect Pin 1 and Pin 5 to ground. Connect Pin 2, Pin 3, Pin 4, and Pin 6 to a 3.3 V power supply.
2. Pin 2, Pin 3, Pin 4, and Pin 6 may be tied together as well as Pin 1 and Pin 5, for ease of use.

SETTING UP THE SIGNAL CONNECTIONS

After setting up the power connections, use the following procedure to set up the signal connections:

1. Connect a 3.3 V CMOS signal, with the intended input frequency, to the reference input (SMA Connector J1, labeled REFA). By default, the reference input of this evaluation board is dc-coupled.
2. The AD9550 does not support a differential input or a secondary input (REFB).
3. Connect a measurement device (such as oscilloscope, spectrum analyzer, or frequency counter) to any of the SMA Connectors J3 through J6. By default, the output signals of the AD9550 evaluation board are ac-coupled with a 100 Ω differential termination.

PROGRAMMING THE AD9550 GUIDELINES

The AD9550 is programmed via pin programming, that is, setting the logic levels on the frequency select pins of the device, which is accomplished by using the DIP switches located on four switch groupings, S1 through S4, located at the bottom right of the AD9550 evaluation board. Within the frequency select pins are three subsets of pins, A[3:0], Y[5:0], and OM[2:0], which together determine the AD9550 operation. The A[3:0] pins define the expected reference input frequency, the Y[5:0] pins define the output frequency, and the OM[2:0] pins define the output drivers. Once the user-defined pin combinations are implemented via the DIP switches and the expected reference input frequency is preset, the $\overline{\text{RESET}}$ pin should be toggled low to high to reset the AD9550, load the part settings defined by the frequency select pins, and assert an autocalibration on the VCO. Note that some A[3:0] and Y[5:0] pin combinations are not compatible or may require the changing of external loop filter components on the evaluation board (described in further detail in the Loop Filter section). To avoid this, verify the chosen frequency select pin combinations with Table 4.

DIP SWITCH PIN CONTROL DESCRIPTIONS

A[3:0] Pins

These pins define a four-digit binary value, which is decoded to a set of predetermined input frequencies, described in Table 2. These pins are located on Switch Group S3.

Y[5:0] Pins

These pins define a six-digit binary value, which is decoded to a set of predetermined output frequencies, described in Table 3. These pins are located across Switch Group S1 and Switch Group S2. Note that the A[3:0] and Y[5:0] pin combination determines the charge pump current and feedback divider of the PLL (see Table 4).

OM[2:0] Pins

These pins define a three-digit binary value, which is decoded to a set of predetermined output driver modes for the two output clocks, described in Table 1. These pins are located on Switch Group S4.

Table 1. Logic Family Assignment via the OM[2:0] Pins

	Logic Family	
OM[2:0]	**OUT1**	**OUT2**
000	LVPECL	LVPECL
001	LVPECL	LVDS
010	LVDS	LVPECL
011	LVPECL	CMOS
100	LVDS	LVDS
101	LVDS	CMOS
110	CMOS	LVDS
111	CMOS	CMOS

RESETB Pin

This pin performs a hard reset of the AD9550. It also asserts an autocalibration of the VCO, though this calibration is only effective if the frequency select pins are set to a valid combination and a valid reference input frequency, as determined by the A[3:0] pins, at the time that RESETB is brought high.

REFB_SEL Pin

The AD9550 supports only one reference input and; therefore, this pin is tied to a logic low state.

Table 2. Pin-Configured Input Frequency, A[3:0] Pins

A[3:0]	f_{REF} (MHz)	Divide-by-5[1]	×2[1]	R (Decimal)
0000	Not used			
0001	0.008	Bypassed	On	1
0010	1.536	Bypassed	Bypassed	96
0011	2.048	Bypassed	Bypassed	128
0100	16.384	Bypassed	Bypassed	1024
0101	19.44	Bypassed	Bypassed	1215
0110 [2]	25	Bypassed	On	3125
0111	38.88	Bypassed	Bypassed	2430
1000	61.44	Bypassed	Bypassed	3840
1001	77.76	Bypassed	Bypassed	4860
1010	122.88	Bypassed	Bypassed	7680
1011	125	On	On	3125
1100	1.544	Bypassed	On	193
1101[3]	155.52	Bypassed	Bypassed	59
1110[4]	25 or 77.76	Bypassed	Bypassed	16
1111	200/3	Bypassed	Bypassed	5000

[1] For divide-by-5 and ×2 frequency scalers, on indicates active.
[2] Using A[3:0] = 0110 to yield a 25 MHz to 125 MHz conversion provides a loop bandwidth of 170 Hz. An alternate 25 MHz to 125 MHz conversion uses A[3:0] = 1110, which provides a loop bandwidth of 20 kHz.
[3] A[3:0] = 1101 only work with Y[5:0] = 101101 through 110010.
[4] A[3:0] = 1110 only work with Y[5:0] = 110011 or 111111.

Table 3. Pin-Configured Output Frequency, Y[5:0] Pins

Y[5:0]	f_{VCO} (MHz)	f_{OUT1} (MHz)	f_{OUT2} (MHz)	P_0	P_1	P_2
000000	Not used					
000001	3686.4	245.76	245.76	5	3	3
000010	3686.4	245.76	122.88	5	3	6
000011	3686.4	245.76	61.44	5	3	12
000100	3686.4	245.76	16.384	5	3	45
000101	3686.4	245.76	2.048	5	3	360
000110	3686.4	245.76	1.536	5	3	480
000111	3686.4	122.88	122.88	5	6	6
001000	3686.4	122.88	61.44	5	6	12
001001	3686.4	122.88	16.384	5	6	45
001010	3686.4	122.88	2.048	5	6	360
001011	3686.4	122.88	1.536	5	6	480
001100	3686.4	61.44	61.44	5	12	12
001101	3686.4	61.44	16.384	5	12	45
001110	3686.4	61.44	2.048	5	12	360
001111	3686.4	61.44	1.536	5	12	480
010000	3686.4	16.384	16.384	5	45	45
010001	3686.4	16.384	2.048	5	45	360
010010	3686.4	16.384	1.536	5	45	480
010011	3686.4	2.048	2.048	5	360	360
010100	3686.4	2.048	1.536	5	360	480
010101	3686.4	1.536	1.536	5	480	480
010110	3750	156.25	156.25	6	4	4
010111	3750	156.25	125	6	4	5
011000	3750	156.25	25	6	4	25
011001	3750	125	125	6	5	5
011010	3750	125	25	6	5	25
011011	3750	25	25	6	25	25
011100	3732.48	155.52	155.52	6	4	4

Y[5:0]	f_{VCO} (MHz)	f_{OUT1} (MHz)	f_{OUT2} (MHz)	P_0	P_1	P_2
011101	3732.48	155.52	77.76	6	4	8
011110	3732.48	155.52	19.44	6	4	32
011111	3732.48	77.76	77.76	6	8	8
100000	3732.48	77.76	19.44	6	8	32
100001	3732.48	19.44	19.44	6	32	32
100010	3686.4	153.6	153.6	6	4	4
100011	3686.4	153.6	122.88	6	4	5
100100	3686.4	153.6	61.44	6	4	10
100101	3686.4	153.6	2.048	6	4	300
100110	3686.4	153.6	1.536	6	4	400
100111	3600	100	100	6	6	6
101000	3600	100	50	6	6	12
101001	3600	100	25	6	6	24
101010	3600	50	50	6	12	12
101011	3600	50	25	6	12	24
101100	3705.6	1.544	1.544	6	400	400
101101	~3985.53	f_O[1]	f_O[1]	6	1	1
101110	~3985.53	f_O[1]	$f_O/2$[1]	6	1	2
101111	~3985.53	f_O[1]	$f_O/4$[1]	6	1	4
110000	~3985.53	$f_O/2$[1]	$f_O/2$[1]	6	2	2
110001	~3985.53	$f_O/2$[1]	$f_O/4$[1]	6	2	4
110010	~3985.53	$f_O/4$[1]	$f_O/4$[1]	6	4	4
110011	3732.48	622.08	622.08	6	1	1
110100 to 111110	Undefined					
111111	3750	125	25	5	6	30

[1] f_O = 39,191.04/59 MHz.

Table 4. Pin Configuration vs. PLL Feedback Divider Value and Charge Pump Value

A[3:0]	Y[5:0]	N[1]	CP[2]
0001 to 1100	000001 to 010101	230,400	121
	010110 to 011011	234,375	121
	011100 to 100001	233,280	121
	100010 to 100110	230,400	121
	100111 to 101011	225,000	121
	101100	231,600	121
	101101 to 111111	Undefined	
1101	000001 to 101100	Undefined	
	101101 to 110010	1512	255
	110010 to 111111	Undefined	
1110	000001 to 110010	Undefined	
	110011	768	121
	110100 to 111110	Undefined	
	111111	2400	121
1111	000001 to 010101	276,480	145
	010110 to 011011	281,250	145
	011100 to 100001	279,936	145
	100010 to 100110	276,480	145
	100111 to 101011	270,000	145
	101100	277,920	145
	101101 to 111111	Undefined	

[1] PLL feedback divider value (decimal).
[2] Charge pump value (decimal). Multiply by 3.5 µA to yield I_{CP}.

LOOP FILTER

The internal portion of the loop filter has two configurations: one is for low loop bandwidth applications (~170 Hz) and the other is for medium (~20 kHz)/high (~75 kHz) bandwidth applications. The low loop bandwidth condition applies when the feedback divider value (N) is 2^{14} (16,384) or greater. Otherwise, the medium/high loop bandwidth configuration is in effect. The feedback divider value depends on the configuration of the A[3:0] and Y[5:0] pins per Table 4.

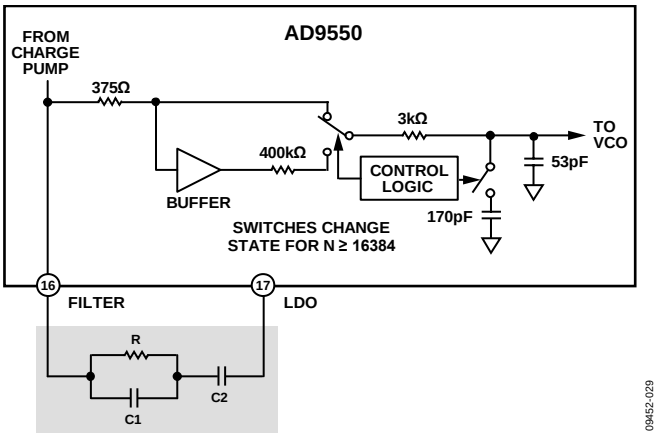

Figure 2. External Loop Filter

The bandwidth of the loop filter primarily depends on three external components: R, C1, and C2 (labeled on the evaluation board as R48, C15, and C3, respectively). There are two sets of recommended values for these components corresponding to the low and medium/high loop bandwidth configurations (see Table 5).

Table 5. External Loop Filter Components

A[3:0] Pins	R	C1	C2	Loop Bandwidth
0001 to 1100 and 1111	6.8 kΩ	47 nF	1 µF	0.17 kHz
1110[1]	12 kΩ	51 pF	220 nF	20 kHz
1101 to 1110	12 kΩ	51 pF	220 nF	75 kHz

[1] The 20 kHz loop bandwidth case only applies when the A[3:0] pins = 1110 and the Y[5:0] pins = 111111.

To achieve the best jitter performance in applications requiring a loop bandwidth of less than 1 kHz, C1 and C2 must have an insulation resistance of at least 500 ΩF.

The evaluation board comes preconfigured with the external loop filter components required for the low loop bandwidth setting. However, it is good practice for any frequency select pin combination to reference Table 5 for loop filter validation. For more detail on the AD9550 loop filter, reference the AD9550 data sheet.

PLL LOCKED INDICATOR

The PLL provides a status indicator (LOCKED) that appears at SMA Connector J2 and LED CR2. When the PLL acquires phase lock, the LOCKED pin switches to a Logic 1 state. When the PLL loses lock, however, the LOCKED pin returns to a Logic 0 state.

USING DIP SWITCHES

1. Determine the desired reference input frequency, output frequencies, and output drivers by referencing Table 2, Table 3, and Table 1 respectively and set the DIP switches appropriately.
2. Reference Table 5 to confirm the preprogrammed loop bandwidth and that the components of the evaluation board external loop filter match those required to the current frequency select pin combination.
3. Set up the power and signal connections to the evaluation board according to the Evaluation Board Hardware section.
4. Toggle the RESETB DIP switch, to apply the pin settings and calibrate the VCO.
5. Confirm that the PLL is locked by observing the lock detect signal via LED CR2 or SMA Connector J2. If this signal is low, confirm the reference input frequency and external loop filter components. If these are correct, initiate another VCO calibration by toggling the RESETB DIP switch again.
6. Observe the output via the connected lab measurement equipment.

NOTES

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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