250 kSPS, 12-Bit Impedance Converter, Network Analyzer

Data Sheet

AD5934

FEATURES

- Programmable output peak-to-peak excitation voltage to a maximum frequency of 100 kHz
- Programmable frequency sweep capability with serial I²C interface
- Frequency resolution of 27 bits (<0.1 Hz)
- Impedance measurement range from 1 kΩ to 10 MΩ
- Capable of measuring 100 Ω to 1 kΩ with additional circuitry
- Phase measurement capability
- System accuracy of 0.5%
- 2.7 V to 5.5 V power supply operation
- Temperature range: −40°C to +125°C
- 16-lead SSOP package

APPLICATIONS

- Electrochemical analysis
- Bioelectrical impedance analysis
- Impedance spectroscopy
- Complex impedance measurement
- Corrosion monitoring and protection equipment
- Biomedical and automotive sensors
- Proximity sensing
- Nondestructive testing
- Material property analysis
- Fuel/battery cell condition monitoring

GENERAL DESCRIPTION

The AD5934 is a high precision impedance converter system solution that combines an on-board frequency generator with a 12-bit, 250 kSPS, analog-to-digital converter (ADC). The frequency generator allows an external complex impedance to be excited with a known frequency. The response signal from the impedance is sampled by the on-board ADC and a discrete Fourier transform (DFT) is processed by an on-board DSP engine. The DFT algorithm returns a real (R) and imaginary (I) data-word at each output frequency.

Once calibrated, the magnitude of the impedance and relative phase of the impedance at each frequency point along the sweep is easily calculated using the following two equations:

$$Magnitude = \sqrt{R^2 + I^2}$$

$$Phase = \tan^{-1}(I/R)$$

A similar device, available from Analog Devices, Inc., is the AD5933, which is a 2.7 V to 5.5 V, 1 MSPS, 12-bit impedance converter, with an internal temperature sensor, available in a 16-lead SSOP.

FUNCTIONAL BLOCK DIAGRAM

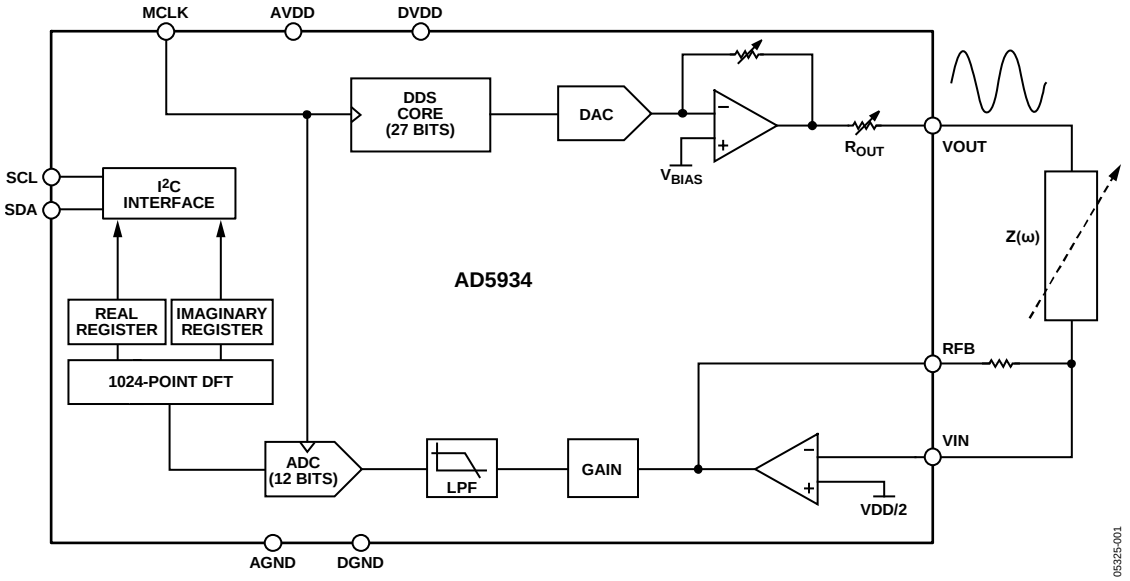

Figure 1.

Rev. C

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AD5934* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD5933 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1053: AD5933 Evaluation Board Example Measurement
- AN-1252: How to Configure the AD5933/AD5934
- AN-1389: Recommended Rework Procedure for the Lead Frame Chip Scale Package (LFCSP)
- AN-237: Choosing DACs for Direct Digital Synthesis
- AN-280: Mixed Signal Circuit Technologies
- AN-342: Analog Signal-Handling for High Speed and Accuracy
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-419: A Discrete, Low Phase Noise, 125 MHz Crystal Oscillator for the AD9850
- AN-423: Amplitude Modulation of the AD9850 Direct Digital Synthesizer
- AN-543: High Quality, All-Digital RF Frequency Modulation Generation with the ADSP-2181 and the AD9850 DDS
- AN-557: An Experimenter's Project:
- AN-587: Synchronizing Multiple AD9850/AD9851 DDS-Based Synthesizers
- AN-605: Synchronizing Multiple AD9852 DDS-Based Synthesizers
- AN-621: Programming the AD9832/AD9835
- AN-632: Provisionary Data Rates Using the AD9951 DDS as an Agile Reference Clock for the ADN2812 Continuous-Rate CDR
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-772: A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)
- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal

- AN-953: Direct Digital Synthesis (DDS) with a Programmable Modulus

Data Sheet

- AD5934: 250KSPS, 12-Bit Impedance Converter, Network Analyzer Data Sheet

Product Highlight

- Impedance-to-Digital Converters—Compact and Easy to Use
- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD5933 IIO Impedance Converter and Network Analyzer Linux Driver
- AD5934 Evaluation Software

REFERENCE DESIGNS

- CN0217

REFERENCE MATERIALS

Technical Articles

- 400-MSample DDSs Run On Only +1.8 VDC
- ADI Buys Korean Mobile TV Chip Maker
- Basics of Designing a Digital Radio Receiver (Radio 101)
- DDS Applications
- DDS Circuit Generates Precise PWM Waveforms
- DDS Design
- DDS Device Produces Sawtooth Waveform
- DDS Device Provides Amplitude Modulation
- DDS IC Initiates Synchronized Signals
- DDS IC Plus Frequency-To-Voltage Converter Make Low-Cost DAC
- DDS Simplifies Polar Modulation
- Digital Potentiometers Vary Amplitude In DDS Devices
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Digital Waveform Generator Provides Flexible Frequency Tuning for Sensor Measurement
- Improved DDS Devices Enable Advanced Comm Systems
- Integrated DDS Chip Takes Steps To 2.7 GHz
- Simple Circuit Controls Stepper Motors
- Speedy A/Ds Demand Stable Clocks
- Synchronized Synthesizers Aid Multichannel Systems
- The Year of the Waveform Generator
- Two DDS ICs Implement Amplitude-shift Keying
- Video Portables and Cameras Get HDMI Outputs

DESIGN RESOURCES

- AD5934 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD5934 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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2/12—Rev. A to Rev. B

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5/8—Rev. 0 to Rev. A

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6/05—Revision 0: Initial Version

SPECIFICATIONS

VDD = 3.3 V, MCLK = 16.776 MHz, 2 V p-p output excitation voltage @ 30 kHz, 200 kΩ connected between Pin 5 and Pin 6; feedback resistor = 200 kΩ connected between Pin 4 and Pin 5; PGA gain = ×1, unless otherwise noted.

Table 1.

	Y Version[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SYSTEM					
Impedance Range	1 k		10 M	Ω	100 Ω to 1 kΩ requires extra buffer circuitry, see Measuring Small Impedances section
Total System Accuracy		0.5		%	2 V p-p output excitation voltage at 30 kHz, 200 kΩ connected between Pin 5 and Pin 6
System Impedance Error Drift		30		ppm/°C	
TRANSMIT STAGE					
Output Frequency Range[2]	1		100	kHz	
Output Frequency Resolution		0.1		Hz	<0.1 Hz resolution achievable using direct digital synthesis (DDS) techniques
MCLK Frequency			16.776	MHz	Maximum system clock frequency
TRANSMIT OUTPUT VOLTAGE					
Range 1					
AC Output Excitation Voltage[3]		1.98		V p-p	Refer to Figure 4 for output voltage distribution
DC Bias[4]		1.48		V	DC bias of the ac excitation signal; see Figure 5
DC Output Impedance		200		Ω	T_A = 25°C
Short-Circuit Current to Ground at VOUT		±5.8		mA	T_A = 25°C
Range 2					
AC Output Excitation Voltage[3]		0.97		V p-p	See Figure 6
DC Bias[4]		0.76		V	DC bias of output excitation signal; see Figure 7
DC Output Impedance		2.4		kΩ	
Short-Circuit Current to Ground at VOUT		±0.25		mA	
Range 3					
AC Output Excitation Voltage[3]		0.383		V p-p	See Figure 8
DC Bias[4]		0.31		V	DC bias of output excitation signal; see Figure 9
DC Output Impedance		1		kΩ	
Short-Circuit Current to Ground at VOUT		±0.20		mA	
Range 4					
AC Output Excitation Voltage[3]		0.198		V p-p	See Figure 10
DC Bias[4]		0.173		V	DC bias of output excitation signal; see Figure 11
DC Output Impedance		600		Ω	
Short-Circuit Current to Ground at VOUT		±0.15		mA	
SYSTEM AC CHARACTERISTICS					
Signal-to-Noise Ratio		60		dB	
Total Harmonic Distortion		−52		dB	
Spurious-Free Dynamic Range					
Wide Band (0 MHz to 1 MHz)		−56		dB	
Narrow Band (±5 kHz)		−85		dB	

Parameter	Y Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
RECEIVE STAGE					
Input Leakage Current		1		nA	To VIN pin
Input Capacitance[5]		0.01		pF	Pin capacitance between VOUT and GND
Feedback Capacitance, C_{FB}		3		pF	Feedback capacitance around current-to-voltage amplifier; appears in parallel with feedback resistor
ANALOG-TO-DIGITAL CONVERTER[5]					
Resolution		12		Bits	
Sampling Rate		250		kSPS	ADC throughput rate
LOGIC INPUTS					
Input High Voltage, V_{IH}	0.7 × VDD				
Input Low Voltage, V_{IL}			0.3 × VDD		
Input Current[6]			1	μA	T_A = 25°
Input Capacitance			7	pF	T_A = 25°C
POWER REQUIREMENTS					
VDD	2.7		5.5	V	
I_{DD}, Normal Mode		10	15	mA	VDD = 3.3 V
		17	25	mA	VDD = 5.5 V
I_{DD}, Standby Mode		7		mA	VDD = 3.3 V; see the Control Register section
		9		mA	VDD = 5.5 V
I_{DD}, Power-Down Mode		0.7	5	μA	VDD = 3.3 V
		1	8	μA	VDD = 5.5 V

[1] Temperature range for Y version = −40°C to +125°C, typical at +25°C.
[2] The lower limit of the output excitation frequency can be lowered by scaling the clock supplied to the AD5934.
[3] The peak-to-peak value of the ac output excitation voltage scales with supply voltage according to the following formula. VDD is the supply voltage.
Output Excitation Voltage (V p-p) = [2/3.3] × *VDD*
[4] The dc bias value of the output excitation voltage scales with supply voltage according to the following formula. VDD is the supply voltage.
Output Excitation Voltage (V p-p) = [2/3.3] × *VDD*
[5] Guaranteed by design or characterization, not production tested. Input capacitance at the VOUT pin is equal to pin capacitance divided by open-loop gain of current-to-voltage amplifier.
[6] The accumulation of the currents into Pin 8, Pin 15, and Pin 16.

I²C SERIAL INTERFACE TIMING CHARACTERISTICS

VDD = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted (see Figure 2).

Table 2.

Parameter[1]	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	µs min	SCL cycle time
t_2	0.6	µs min	t_{HIGH}, SCL high time
t_3	1.3	µs min	t_{LOW}, SCL low time
t_4	0.6	µs min	$t_{HD, STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU, DAT}$, data setup time
t_6[2]	0.9	µs max	$t_{HD, DAT}$, data hold time
	0	µs min	$t_{HD, DAT}$, data hold time
t_7	0.6	µs min	$t_{SU, STA}$, setup time for repeated start
t_8	0.6	µs min	$t_{SU, STO}$, stop condition setup time
t_9	1.3	µs min	t_{BUF}, bus free time between a stop and a start condition
t_{10}	300	ns max	t_R, rise time of SDA when transmitting
	0	ns min	t_R, rise time of SCL and SDA when receiving (CMOS compatible)
t_{11}	300	ns max	t_F, fall time of SCL and SDA when transmitting
	0	ns min	t_F, fall time of SDA when receiving (CMOS compatible)
	250	ns max	t_F, fall time of SDA when receiving
	$20 + 0.1\ C_b$[3]	ns min	t_F, fall time of SCL and SDA when transmitting
C_b	400	pF max	Capacitive load for each bus line

[1] Guaranteed by design and characterization, not production tested.
[2] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to $V_{IH\ MIN}$ of the SCL signal) to bridge the undefined falling edge of SCL.
[3] C_b is the total capacitance of one bus line in pF. Note that t_R and t_F are measured between 0.3 VDD and 0.7 VDD.

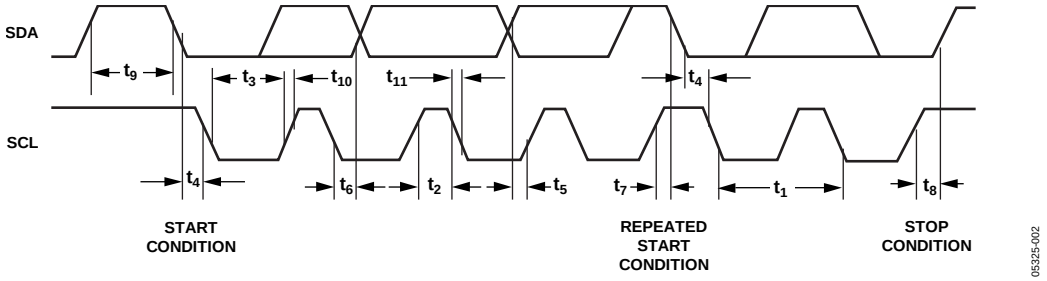


Figure 2. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

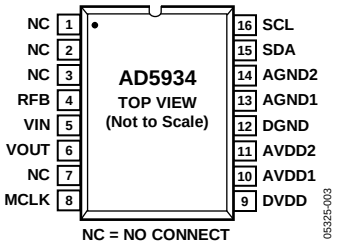
Parameter	Rating
DVDD to GND	−0.3 V to +7.0 V
AVDD1 to GND	−0.3 V to +7.0 V
AVDD2 to GND	−0.3 V to +7.0 V
SDA/SCL to GND	−0.3 V to VDD + 0.3 V
VOUT to GND	−0.3 V to VDD + 0.3 V
VIN to GND	−0.3 V to VDD + 0.3 V
MCLK to GND	−0.3 V to VDD + 0.3 V
Operating Temperatures	
Extended Industrial Range (Y Grade)	−40°C to +125°C
Storage Temperature Range	−65°C to +160°C
Maximum Junction Temperature	150°C
SSOP Package, Thermal Impedance	
θ_{JA}	139°C/W
θ_{JC}	136°C/W
Reflow Soldering (Pb-Free)	
Peak Temperature	260°C
Time at Peak Temperature	10 sec to 40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES:
1. IT IS RECOMMENDED TO TIE ALL SUPPLY CONNECTIONS (PIN 9, PIN 10, AND PIN 11) AND RUN FROM A SINGLE SUPPLY BETWEEN 2.7V AND 5.5V.
2. IT IS ALSO RECOMMENDED TO CONNECT ALL GROUND SIGNALS TOGETHER (PIN 12, PIN 13, AND PIN 14).

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 3, 7	NC	No Connect. Do not connect to this pin.
4	RFB	External Feedback Resistor. Connect from Pin 4 to Pin 5. This pin sets the gain of the current-to-voltage amplifier on the receive side.
5	VIN	Input to Receive Transimpedance Amplifier. VIN presents a virtual earth voltage of VDD/2.
6	VOUT	Excitation Voltage Signal Output.
8	MCLK	The master clock for the system is supplied by the user.
9	DVDD	Digital Supply Voltage.
10	AVDD1	Analog Supply Voltage 1. Used for powering the analog core.
11	AVDD2	Analog Supply Voltage 2. Used for internal references.
12	DGND	Digital Ground.
13	AGND1	Analog Ground 1.
14	AGND2	Analog Ground 2.
15	SDA	I^2C® Data Input.
16	SCL	I^2C Clock Input.

TYPICAL PERFORMANCE CHARACTERISTICS

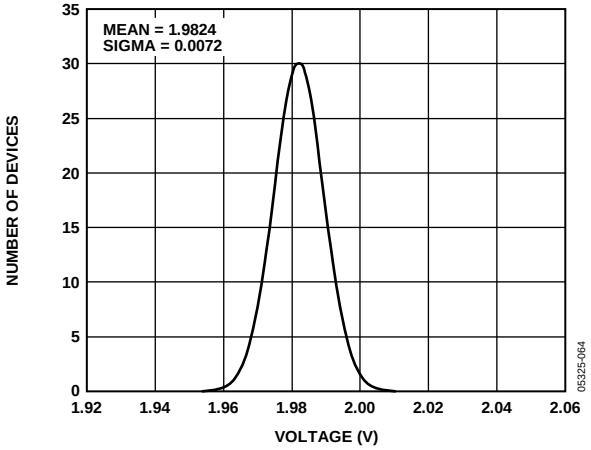


Figure 4. Range 1 Output Excitation Voltage Distribution, VDD = 3.3 V

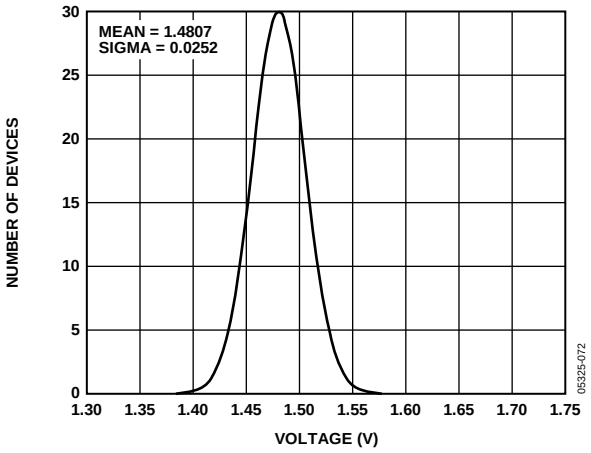


Figure 5. Range 1 DC Bias Distribution, VDD = 3.3 V

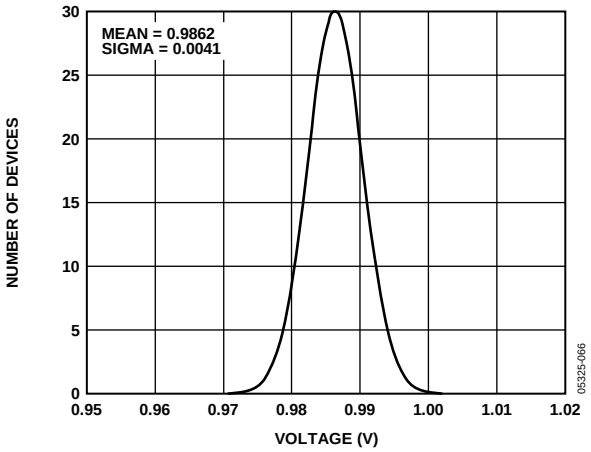


Figure 6. Range 2 Output Excitation Voltage Distribution, VDD = 3.3 V

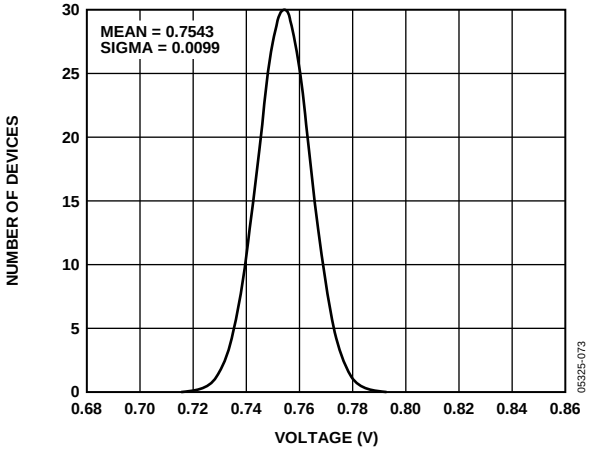


Figure 7. Range 2 DC Bias Distribution, VDD = 3.3 V

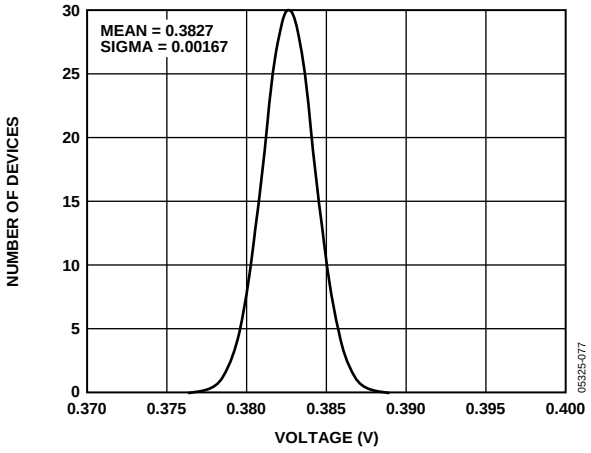


Figure 8. Range 3 Output Excitation Voltage Distribution, VDD = 3.3 V

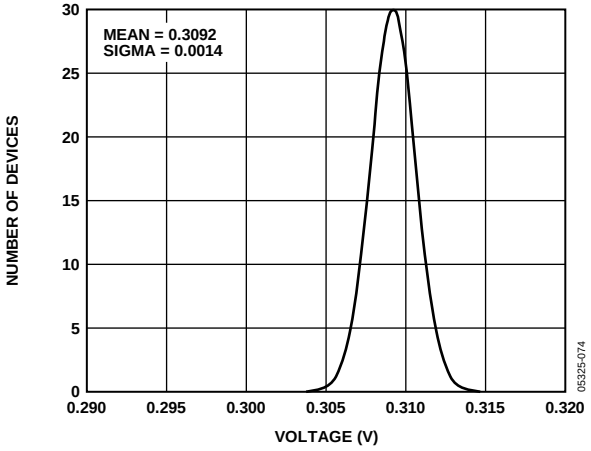


Figure 9. Range 3 DC Bias Distribution, VDD = 3.3 V

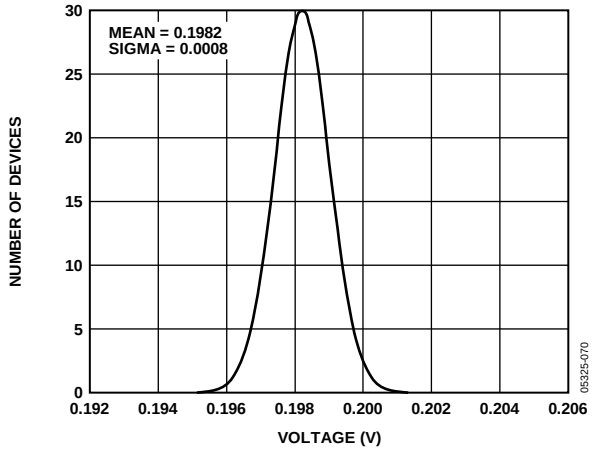


Figure 10. Range 4 Output Excitation Voltage Distribution, VDD = 3.3 V

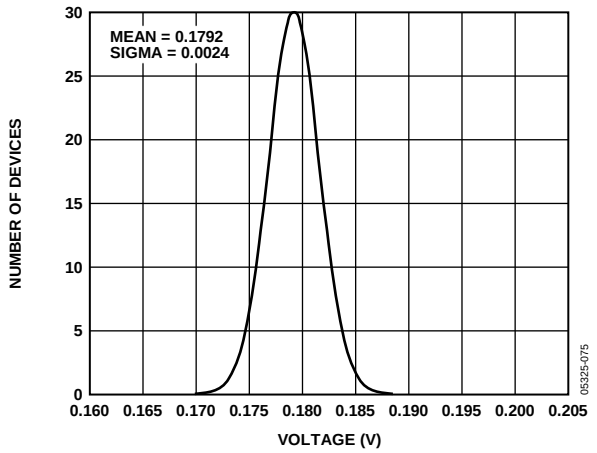


Figure 11. Range 4 DC Bias Distribution, VDD = 3.3 V

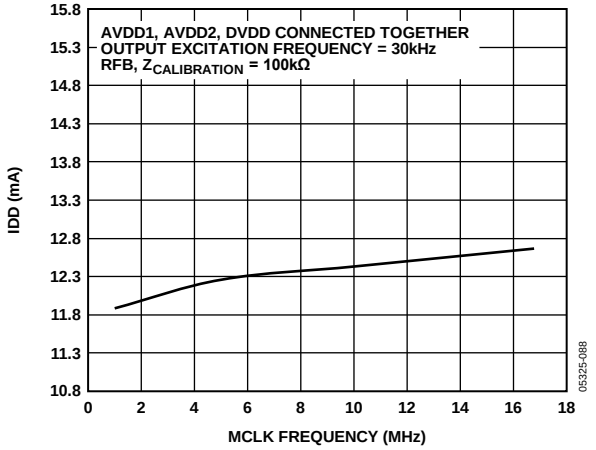


Figure 12. Typical Supply Current (IDD) vs. MCLK Frequency

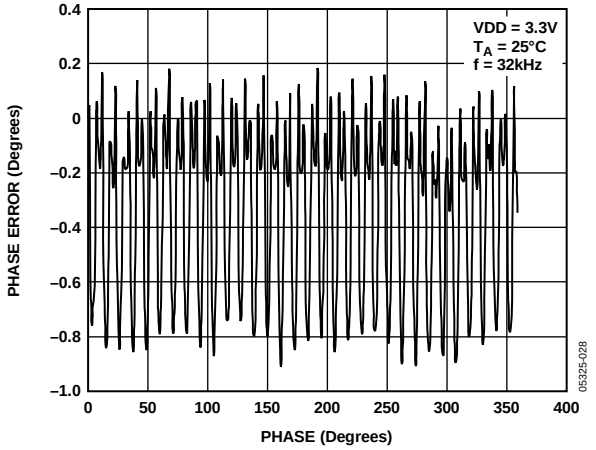


Figure 13. Typical Phase Error

TERMINOLOGY

Total System Accuracy

The AD5934 can accurately measure a range of impedance values to less than 0.5% of the correct impedance value for supply voltages between 2.7 V to 5.5 V.

Spurious-Free Dynamic Range (SFDR)

Along with the frequency of interest, harmonics of the fundamental frequency and images of these frequencies are present at the output of a DDS device. The spurious-free dynamic range refers to the largest spur or harmonic present in the band of interest. The wideband SFDR gives the magnitude of the largest harmonic or spur relative to the magnitude of the fundamental frequency in the 0 Hz to Nyquist bandwidth. The narrow-band SFDR gives the attenuation of the largest spur or harmonic in a bandwidth of ±200 kHz, about the fundamental frequency.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of harmonics to the fundamental, where V1 is the rms amplitude of the fundamental, and V2, V3, V4, V5, and V6 are the rms amplitudes of the second through the sixth harmonics. THD is defined as

$$THD(\text{dB}) = 20 \log \frac{\sqrt{V2^2 + V3^2 + V4^2 + V5^2 + V6^2}}{V1}$$

SYSTEM DESCRIPTION

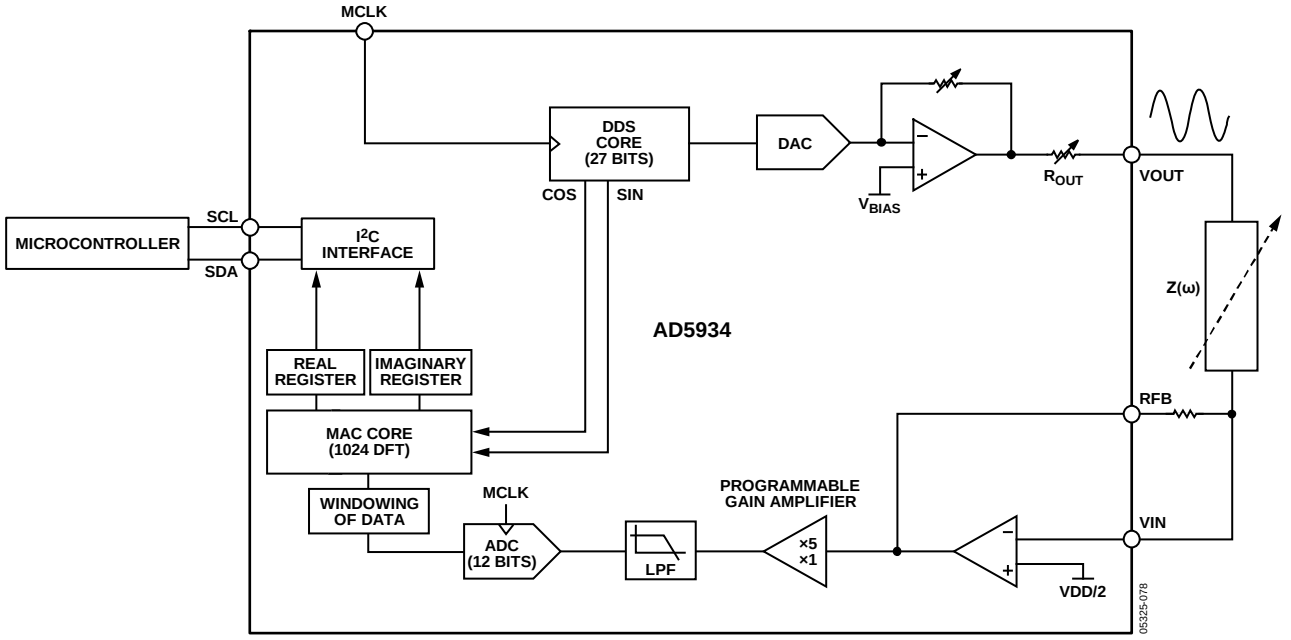


Figure 14. Block Overview

The AD5934 is a high precision, impedance converter system solution that combines an on-board frequency generator with a 12-bit, 250 kSPS ADC. The frequency generator allows an external complex impedance to be excited with a known frequency. The response signal from the impedance is sampled by the on-board ADC and DFT processed by an on-board DSP engine. The DFT algorithm returns both a real (R) and imaginary (I) data-word at each frequency point along the sweep. The impedance magnitude and phase is easily calculated using the following equations:

$$Magnitude = \sqrt{R^2 + I^2}$$

$$Phase = \tan^{-1}(I/R)$$

To characterize an impedance profile Z(ω), generally a frequency sweep is required such as that shown in Figure 15.

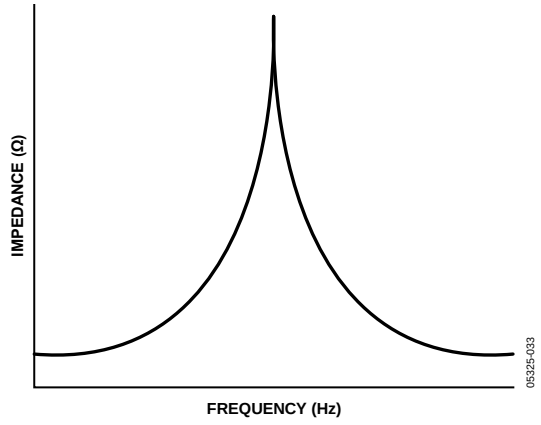


Figure 15. Impedance vs. Frequency Profile

The AD5934 permits the user to perform a frequency sweep with a user-defined start frequency, frequency resolution, and number of points in the sweep. In addition, the device allows the user to program the peak-to-peak value of the output sinusoidal signal as an excitation to the external unknown impedance connected between the VOUT and VIN pins.

Table 5 gives the four possible output peak-to-peak voltages and the corresponding dc bias levels for each range for 3.3 V. These values are ratiometric with VDD. So for a 5 V supply:

$$Output\ Excitation\ Voltage\ for\ Range\ 1 = 1.98 \times \frac{5.0}{3.3} = 3\ \text{V p-p}$$

$$Output\ DC\ Bias\ Voltage\ for\ Range\ 1 = 1.48 \times \frac{5.0}{3.3} = 2.24\ \text{V p-p}$$

Table 5. Voltage Levels Respective Bias Levels for 3.3 V

Range No.	Output Excitation Voltage Amplitude	Output DC Bias Level
1	1.98 V p-p	1.48 V
2	0.99 V p-p	0.74 V
3	383 mV p-p	0.31 V
4	198 mV p-p	0.179 V

The excitation signal for the transmit stage is provided on-chip using DDS techniques that permit subhertz resolution. The receive stage receives the input signal current from the unknown impedance, performs signal processing, and digitizes the result. The clock for the DDS is generated from an external reference clock that is provided by the user at MCLK.

TRANSMIT STAGE

As shown in Figure 16, the transmit stage of the AD5934 is made up of a 27-bit phase accumulator DDS core that provides the output excitation signal at a particular frequency. The input to the phase accumulator is taken from the contents of the start frequency register (see Register Address 0x82, Register Address 0x83, and Register Address 0x84). Although the phase accumulator offers 27 bits of resolution, the start frequency register has the three most significant bits (MSBs) set to 0 internally; therefore, the user has the ability to program only the lower 24 bits of the start frequency register.

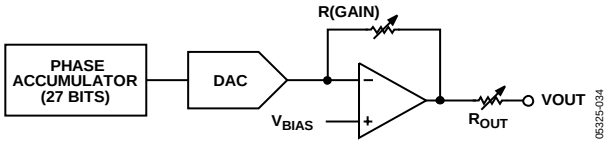


Figure 16. Transmit Stage

The AD5934 offers a frequency resolution programmable by the user down to 0.1 Hz. The frequency resolution is programmed via a 24-bit word loaded serially over the I^2C interface to the frequency increment register.

The frequency sweep is fully described by the programming of three parameters: the start frequency, the frequency increment, and the number of increments.

Start Frequency

This is a 24-bit word that is programmed to the on-board RAM at Register Address 0x82, Register Address 0x83, and Register Address 0x84 (see the Register Map section). The required code loaded to the start frequency register is the result of the formula shown in Equation 1, based on the master clock frequency and the required start frequency output from the DDS.

$$Start\ Frequency\ Code = \left(\frac{Required\ Output\ Start\ Frequency}{\frac{MCLK}{16}} \right) \times 2^{27} \quad (1)$$

For example, if the user requires the sweep to begin at 30 kHz and has a 16 MHz clock signal connected to MCLK, the code that needs to be programmed is given by

$$Start\ Frequency\ Code = \left(\frac{30\ \text{kHz}}{\left(\frac{16\ \text{MHz}}{16} \right)} \right) \times 2^{27} = 0\text{x}3\text{D}70\text{A}3$$

The user programs the value of 0x3D to Register Address 0x82, the value 0x70 to Register Address 0x83, and the value 0xA3 to Register Address 0x84.

Frequency Increment

This is a 24-bit word that is programmed to the on-board RAM at Register Address 0x85, Register Address 0x86, and Register Address 0x87 (see the Register Map section). The required code loaded to the frequency increment register is the result of the formula shown in Equation 2, based on the master clock frequency and the required increment frequency output from the DDS.

$$Frequency\ Increment\ Code = \left(\frac{Required\ Frequency\ Increment}{\frac{MCLK}{16}} \right) \times 2^{27} \quad (2)$$

For example, if the user requires the sweep to have a resolution of 10 Hz and has a 16 MHz clock signal connected to MCLK, the code that needs to be programmed is given by

$$Frequency\ Increment\ Code = \left(\frac{10\ \text{Hz}}{\left(\frac{16\ \text{MHz}}{16} \right)} \right) \equiv 0\text{x}00053\text{E}$$

The user programs the value 0x00 to Register Address 0x85, the value 0x05 to Register Address 0x86, and the value 0x3E to Register Address 0x87.

Number of Increments

This is a 9-bit word that represents the number of frequency points in the sweep. The number is programmed to the on-board RAM at Register Address 0x88 and Register Address 0x89 (see the Register Map section). The maximum number of points that can be programmed is 511.

For example, if the sweep needs 150 points, the user programs the value 0x00 to Register Address 0x88 and the value 0x96 to Register Address 0x89.

Once the three parameter values are programmed, the sweep is initiated by issuing a start frequency sweep command to the control register at Register Address 0x80 and Register Address 0x81 (see the Register Map section). Bit D2 in the status register (Register Address 0x8F) indicates the completion of the frequency measurement for each sweep point. Incrementing to the next frequency sweep point is under the control of the user. The measured result is stored in the two register groups that follow: 0x94, 0x95 (real data) and 0x96, 0x97 (imaginary data) that should be read before issuing an increment frequency command to the control register to move to the next sweep point. There is the facility to repeat the current frequency point measurement by issuing a repeat frequency command to the control register. This has the benefit of allowing the user to average successive readings. When the frequency sweep has completed all frequency points, Bit D3 in the status register is set, indicating the completion of the sweep. Once this bit is set, further increments are disabled.

FREQUENCY SWEEP COMMAND SEQUENCE

The following sequence must be followed to implement a frequency sweep:

1. Enter standby mode. Prior to issuing a start frequency sweep command, the device must be placed in standby mode by issuing an enter standby mode command to the control register (Register Address 0x80 and Register Address 0x81). In this mode, the VOUT and VIN pins are connected internally to ground so there is no dc bias across the external impedance or between the impedance and ground.
2. Enter initialize mode. In general, high Q complex circuits require a long time to reach steady state. To facilitate the measurement of such impedances, this mode allows the user full control of the settling time requirement before entering start frequency sweep mode where the impedance measurement takes place.

   An initialize with start frequency command to the control register enters initialize mode. In this mode, the impedance is excited with the programmed start frequency but no measurement takes place. The user times out the required settling time before issuing a start frequency sweep command to the control register to enter the start frequency sweep mode.
3. Enter start frequency sweep mode. The user enters this mode by issuing a start frequency sweep command to the control register. In this mode, the ADC starts measuring after the programmed number of settling time cycles elapses. The user can program an integer number of output frequency cycles (settling time cycles) to Register Address 0x8A and Register Address 0x8B before beginning the measurement at each frequency point (see Figure 24).

   The DDS output signal is passed through a programmable gain stage to generate the four ranges of peak-to-peak output excitation signals listed in Table 5. The peak-to-peak output excitation voltage is selected by setting Bit D10 and Bit D9 in the control register (see the Control Register section) and is made available at the VOUT pin.

RECEIVE STAGE

The receive stage comprises a current-to-voltage amplifier, followed by a programmable gain amplifier (PGA), antialiasing filter, and ADC. The receive stage schematic is shown in Figure 17. The unknown impedance is connected between the VOUT and VIN pins. The first stage current-to-voltage amplifier configuration means that a voltage present at the VIN pin is a virtual ground with a dc value set at VDD/2. The signal current that is developed across the unknown impedance flows into the VIN pin and develops a voltage signal at the output of the current-to-voltage converter. The gain of the current-to voltage amplifier is determined by a user-selectable feedback resistor connected between Pin 4 (RFB) and Pin 5 (VIN). It is important for the user to choose a feedback resistance value which, in conjunction with the selected gain of the PGA stage, maintains the signal within the linear range of the ADC (0 V to VDD).

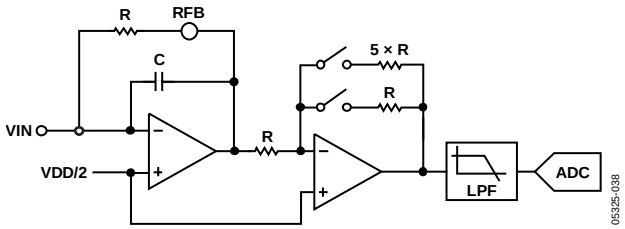


Figure 17. Receive Stage

The PGA allows the user to gain the output of the current-to-voltage amplifier by a factor of 5 or 1 depending upon the status of Bit D8 in the control register (see the Register Map section Register Address 0x80). The signal is then low-pass filtered and presented to the input of the 12-bit, 250 kSPS ADC.

The digital data from the ADC is passed directly to the DSP core of the AD5934 that performs a DFT on the sampled data.

DFT OPERATION

A DFT is calculated for each frequency point in the sweep. The AD5934 DFT algorithm is represented by

$$X(f) = \sum_{n=0}^{1023} \left(x(n)(\cos(n) - j\sin(n)) \right)$$

where:
$X(f)$ is the power in the signal at the Frequency Point f.
$x(n)$ is the ADC output.
$\cos(n)$ and $\sin(n)$ are the sampled test vectors provided by the DDS core at the Frequency f.

The multiplication is accumulated over 1024 samples for each frequency point. The result is stored in two 16-bit registers representing the real and imaginary components of the result. The data is stored in twos complement format.

IMPEDANCE CALCULATION

MAGNITUDE CALCULATION

The first step in the impedance calculation for each frequency point is to calculate the magnitude of the DFT at that point.

The DFT magnitude is given by

$$Magnitude = \sqrt{R^2 + I^2}$$

where:
R is the real number stored at Register Address 0x94 and Register Address 0x95.
I is the imaginary number stored at Register Address 0x96 and Register Address 0x97.

For example, assume the results in the real data and imaginary data registers are as follows at a frequency point:

Real Data Register = 0x038B = 907 decimal

Imaginary Data Register = 0x0204 = 516 decimal

$$Magnitude = \sqrt{(907^2 + 516^2)} = 1043.506$$

To convert this number into impedance, it must be multiplied by a scaling factor called the gain factor. The gain factor is calculated during the calibration of the system with a known impedance connected between the VOUT and VIN pins.

Once the gain factor is calculated, it can be used in the calculation of any unknown impedance between the VOUT and VIN pins.

GAIN FACTOR CALCULATION

An example of a gain factor calculation follows, with these assumptions:

Output excitation voltage = 2 V p-p
Calibration impedance value, $Z_{CALIBRATION}$ = 200 kΩ
PGA gain = ×1
Current-to-voltage amplifier gain resistor = 200 kΩ
Calibration frequency = 30 kHz

The typical contents of the real data and imaginary data registers after a frequency point conversion would then be

Real Data Register = 0xF064 = −3996 decimal

Imaginary Data Register = 0x227E = +8830 decimal

$$Magnitude = \sqrt{(-3996)^2 + (8830)^2} = 9692.106$$

Gain Factor =

$$\left(\frac{Admittance}{Code}\right) = \frac{\left(\frac{1}{Impedance}\right)}{Magnitude}$$

$$Gain\ Factor = \left(\frac{\frac{1}{200\ \text{k}\Omega}}{9692.106}\right) = 515.819 \times 10^{-12}$$

IMPEDANCE CALCULATION USING GAIN FACTOR

The next example illustrates how the calculated gain factor derived previously is used to measure an unknown impedance. For this example, assume that the unknown impedance is 510 kΩ.

After measuring the unknown impedance at a frequency of 30 kHz, assume that the real data and imaginary data registers contain the following data:

Real Data Register = 0xFA3F = −1473 decimal

Imaginary Data Register = 0x0DB3 = +3507 decimal

$$Magnitude = \sqrt{((-1473)^2 + (3507)^2)} = 3802.863$$

The measured impedance at the frequency point is then given by

$$Impedance = \frac{1}{Gain\ Factor \times Magnitude}$$

$$= \frac{1}{515.819273 \times 10^{-12} \times 3802.863}\ \Omega = 509.791\ \text{k}\Omega$$

GAIN FACTOR VARIATION WITH FREQUENCY

Because the AD5934 has a finite frequency response, the gain factor also shows a variation with frequency. This variation in gain factor results in an error in the impedance calculation over a frequency range. Figure 18 shows an impedance profile based on a single-point gain factor calculation. To minimize this error, the frequency sweep should be limited to as small a frequency range as possible.

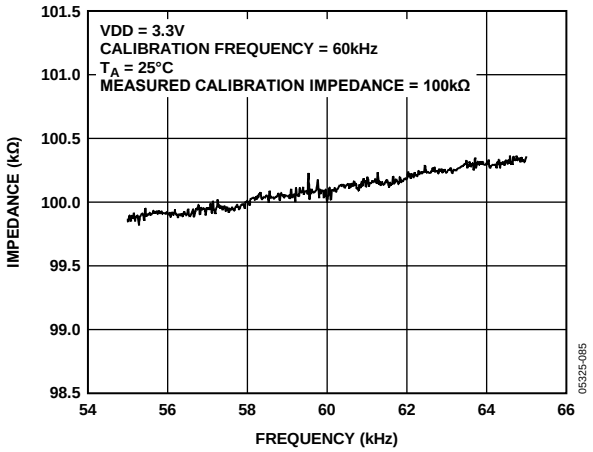


Figure 18. Impedance Profile Using a Single-Point Gain Factor Calculation

2-POINT CALIBRATION

Alternatively, it is possible to minimize this error by assuming that the frequency variation is linear and adjusting the gain factor with a 2-point calibration. Figure 19 shows an impedance profile based on a 2-point gain factor calculation.

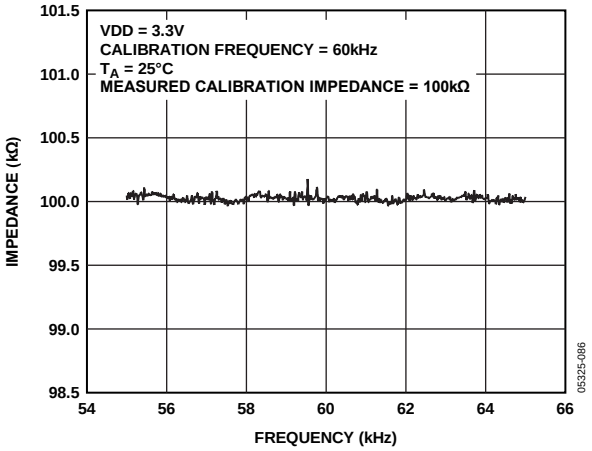


Figure 19. Impedance Profile Using a 2-Point Gain Factor Calculation

2-POINT GAIN FACTOR CALCULATION

This is an example of a 2-point gain factor calculation assuming the following:

Output excitation voltage = 2 V p-p
Calibration impedance value, $Z_{UNKNOWN}$ = 100.0 kΩ
PGA gain = ×1
Supply voltage = 3.3 V
Current-to-voltage amplifier gain resistor = 100 kΩ
Calibration frequencies = 55 kHz and 65 kHz

Typical values of the gain factor calculated at the two calibration frequencies read

Gain factor calculated at 55 kHz is 1.031224×10^{-9}.
Gain factor calculated at 65 kHz is 1.035682×10^{-9}.
Difference in gain factor (ΔGF) is
$1.035682 \times 10^{-9} - 1.031224 \times 10^{-9} = 4.458000 \times 10^{-12}$.
Frequency span of sweep (ΔF) is 10 kHz.

Therefore, the gain factor required at 60 kHz is given by

$$\left(\frac{4.458000\text{E-}12}{10\,\text{kHz}} \times 5\,\text{kHz}\right) + 1.031224 \times 10^{-9}$$

The required gain factor is 1.033453×10^{-9}.

The impedance is calculated as previously described in the Impedance Calculation section.

GAIN FACTOR SETUP CONFIGURATION

When calculating the gain factor, it is important that the receive stage is operating in its linear region. This requires careful selection of the excitation signal range, current-to-voltage gain resistor and PGA gain. The gain through the system shown in Figure 20 is given by

$$\text{Output Excitation Voltage Range} \times \frac{\text{Gain Setting Resistor}}{Z_{UNKNOWN}} \times \text{PGA Gain}$$

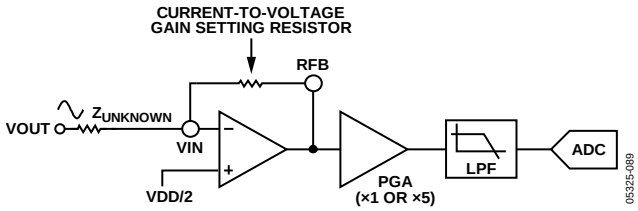


Figure 20. System Voltage Gain

For this example, assume the following system settings:

VDD = 3.3 V
Gain setting resistor = 200 kΩ
$Z_{UNKNOWN}$ = 200 kΩ
PGA setting = ×1

The peak-to-peak voltage presented to the ADC input is 2 V p-p. However, had the user chosen a PGA gain of ×5, the voltage would saturate the ADC.

GAIN FACTOR RECALCULATION

The gain factor must be recalculated for a change in any of the following parameters:

- Current-to-voltage gain setting resistor
- Output excitation voltage
- PGA gain

GAIN FACTOR TEMPERATURE VARIATION

The typical impedance error variation with temperature is in the order of 30 ppm/°C. Figure 21 shows an impedance profile with a variation in temperature for 100 kΩ impedance using a 2-point gain factor calibration.

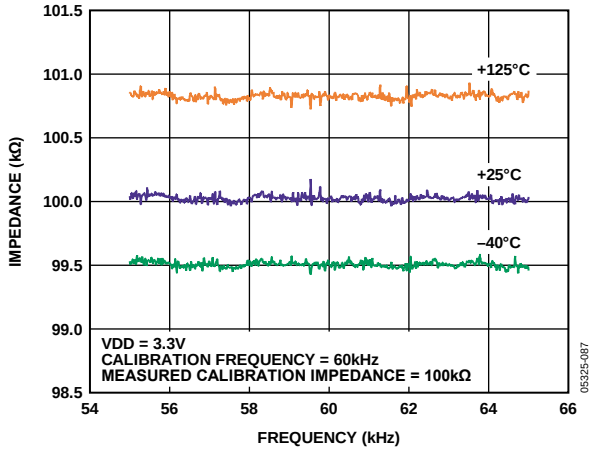


Figure 21. Impedance Profile Variation with Temperature Using a 2-Point Gain Factor Calibration

IMPEDANCE ERROR

Refer to Circuit Note CN-0217 on the AD5933 product page, which highlights a method to improve accuracy. The EVAL-AD5933EBZ board can be used to evaluate the AD5934 performance.

MEASURING THE PHASE ACROSS AN IMPEDANCE

The AD5934 returns a complex output code made up of a separate real and imaginary components. The real component is stored at Register Address 0x94 and Register Address 0x95, and the imaginary component is stored at Register Address 0x96 and Register Address 0x97 after each sweep measurement. These correspond to the real and imaginary components of the DFT and not the resistive and reactive components of the impedance under test.

For example, it is a common misconception to assume that if a user was analyzing a series RC circuit that the real value stored in Register Address 0x94 and Register Address 0x95 and the imaginary value stored in Register Address 0x96 and Register Address 0x97 would correspond to the resistance and capacitive reactance, respectfully. However, this is incorrect because the magnitude of the impedance (|Z|) can be calculated by calculating the magnitude of the real and imaginary components of the DFT given by the following formula:

$$Magnitude = \sqrt{R^2 + I^2}$$

After each measurement, multiply it by the calibration term and invert the product. Therefore, the magnitude of the impedance is given by the following formula:

$$Impedance = \frac{1}{Gain\ Factor \times Magnitude}$$

Where the gain factor is given by

$$Gain\ Factor = \left(\frac{Admittance}{Code}\right) = \frac{\left(\frac{1}{Impedance}\right)}{Magnitude}$$

The user must calibrate the AD5934 system for a known impedance range to determine the gain factor before any valid measurement can take place. Therefore, the user must know the impedance limits of the complex impedance ($Z_{UNKNOWN}$) for the sweep frequency range of interest. The gain factor is simply determined by placing a known impedance between the input/output of the AD5934 and measuring the resulting magnitude of the code. The AD5934 system gain settings need to be chosen to place the excitation signal in the linear region of the on-board ADC.

Because the AD5934 returns a complex output code made up of real and imaginary components, the user is also able to calculate the phase of the response signal through the signal path of the AD5934. The phase is given by the following formula:

$$Phase\ (\text{rads}) = \tan^{-1}(I/R) \quad (3)$$

The phase measured by Equation 3 accounts for the phase shift introduced to the DDS output signal as it passes through the internal amplifiers on the transmit and receive side of the AD5934, along with the low-pass filter, and also the impedance connected between the VOUT and VIN pins of the AD5934.

The parameters of interest for many users are the magnitude of the impedance ($|Z_{UNKNOWN}|$) and the impedance phase (ZØ).The measurement of the impedance phase (ZØ) is a 2-step process.

The first step involves calculating the AD5934 system phase. The AD5934 system phase can be calculated by placing a resistor across the VOUT and VIN pins of the AD5934 and calculating the phase (using Equation 3) after each measurement point in the sweep. By placing a resistor across the VOUT and VIN pins, there is no additional phase lead or lag introduced to the AD5934 signal path, and the resulting phase is due entirely to the internal poles of the AD5934, that is, the system phase.

Once the system phase is calibrated using a resistor, the second step involves calculating the phase of any unknown impedance can be calculated by inserting the unknown impedance between the VIN and VOUT terminals of the AD5934 and recalculating the new phase (including the phase due to the impedance) using the same formula. The phase of the unknown impedance (ZØ) is given by

$$ZØ = (Φunknown - \nabla system)$$

where:

$\nabla system$ is the phase of the system with a calibration resistor connected between VIN and VOUT.

$Φunknown$ is the phase of the system with the unknown impedance connected between VIN and VOUT.

ZØ is the phase due to the impedance, that is, the impedance phase.

Note that it is possible to calculate the gain factor and to calibrate the system phase using the same real and imaginary component values when a resistor is connected between the VOUT and VIN pins of the AD5934, for example, measuring the impedance phase (ZØ) of a capacitor.

The excitation signal current leads the excitation signal voltage across a capacitor by −90 degrees. Therefore, an approximate −90 degrees phase difference between the system phase responses measured with a resistor and the system phase responses measured with a capacitive impedance exists.

As previously outlined, if the user wants to determine the phase angle of the capacitive impedance (ZØ), the user first must determine the system phase response (Vsystem) and subtract this from the phase calculated with the capacitor connected between VOUT and VIN (Φunknown).

Figure 22 shows the AD5934 system phase response calculated using a 220 kΩ calibration resistor (R_{FB} = 220 kΩ, PGA = ×1) and the repeated phase measurement with a 10 pF capacitive impedance.

One important point to note about the phase formula used to plot Figure 22 is that it uses the arctangent function that returns a phase angle in radians and, therefore, it is necessary to convert from radians to degrees.

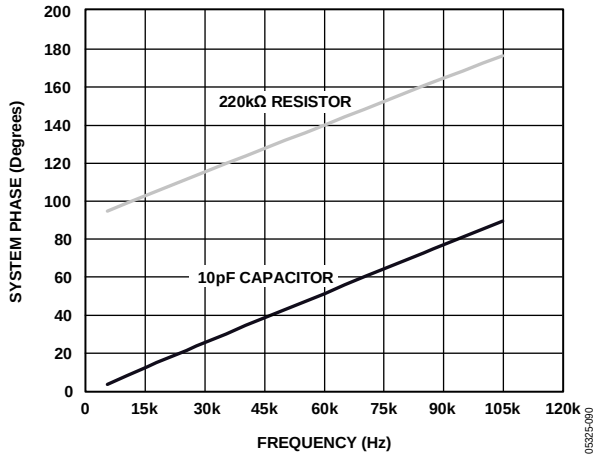


Figure 22. System Phase Response vs. Capacitive Phase

The phase difference (that is, ZØ) between the phase response of a capacitor and the system phase response using a resistor is the impedance phase of the capacitor (ZØ) and is shown in Figure 23.

In addition, when using the real and imaginary values to interpret the phase at each measurement point, care should be taken when using the arctangent formula. The arctangent function only returns the correct standard phase angle when the sign of the real and imaginary values are positive, that is, when the coordinates lie in the first quadrant. The standard angle is taken counterclockwise from the positive real x-axis. If the sign of the real component is positive and the sign of the imaginary component is negative, that is, the data lies in the second quadrant, the arctangent formula returns a negative angle, and it is necessary to add an additional 180° to calculate the correct standard angle. Likewise, when the real and imaginary components are both negative, that is, when data lies in the third quadrant, the arctangent formula returns a positive angle, and it is necessary to add an additional 180° to calculate the correct standard phase. When the real component is positive and the imaginary component is negative, that is, the data lies in the fourth quadrant, the arctangent formula returns a negative angle, and it is necessary to add an additional 360° to calculate the correct standard phase.

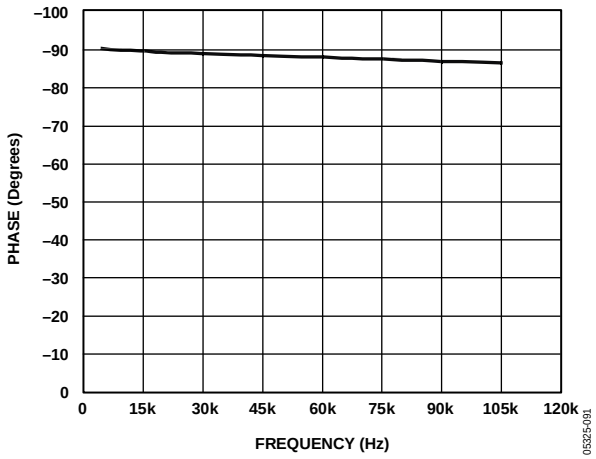


Figure 23. Phase Response of a Capacitor

Therefore, the correct standard phase angle is dependent upon the sign of the real and imaginary components, which is summarized in Table 6.

Table 6. Phase Angle

Real	Imaginary	Quadrant	Phase Angle
Positive	Positive	First	$\tan^{-1}(I/R)\times\frac{180°}{\pi}$
Positive	Negative	Second	$180° + \left(\tan^{-1}(I/R)\times\frac{180°}{\pi}\right)$
Negative	Negative	Third	$180° + \left(\tan^{-1}(I/R)\times\frac{180°}{\pi}\right)$
Negative	Positive	Fourth	$360° + \left(\tan^{-1}(I/R)\times\frac{180°}{\pi}\right)$

Once the magnitude of the impedance (|Z|) and the impedance phase angle (ZØ, in radians) are correctly calculated, it is possible to determine the magnitude of the real (resistive) and imaginary (reactive) components of the impedance ($Z_{UNKNOWN}$) by the vector projection of the impedance magnitude onto the real and imaginary impedance axis using the following formulas:

The real component is given by

$$|Z_{REAL}| = |Z| \times \cos(Z\text{Ø})$$

The imaginary component is given by

$$|Z_{IMAG}| = |Z| \times \sin(Z\text{Ø})$$

PERFORMING A FREQUENCY SWEEP

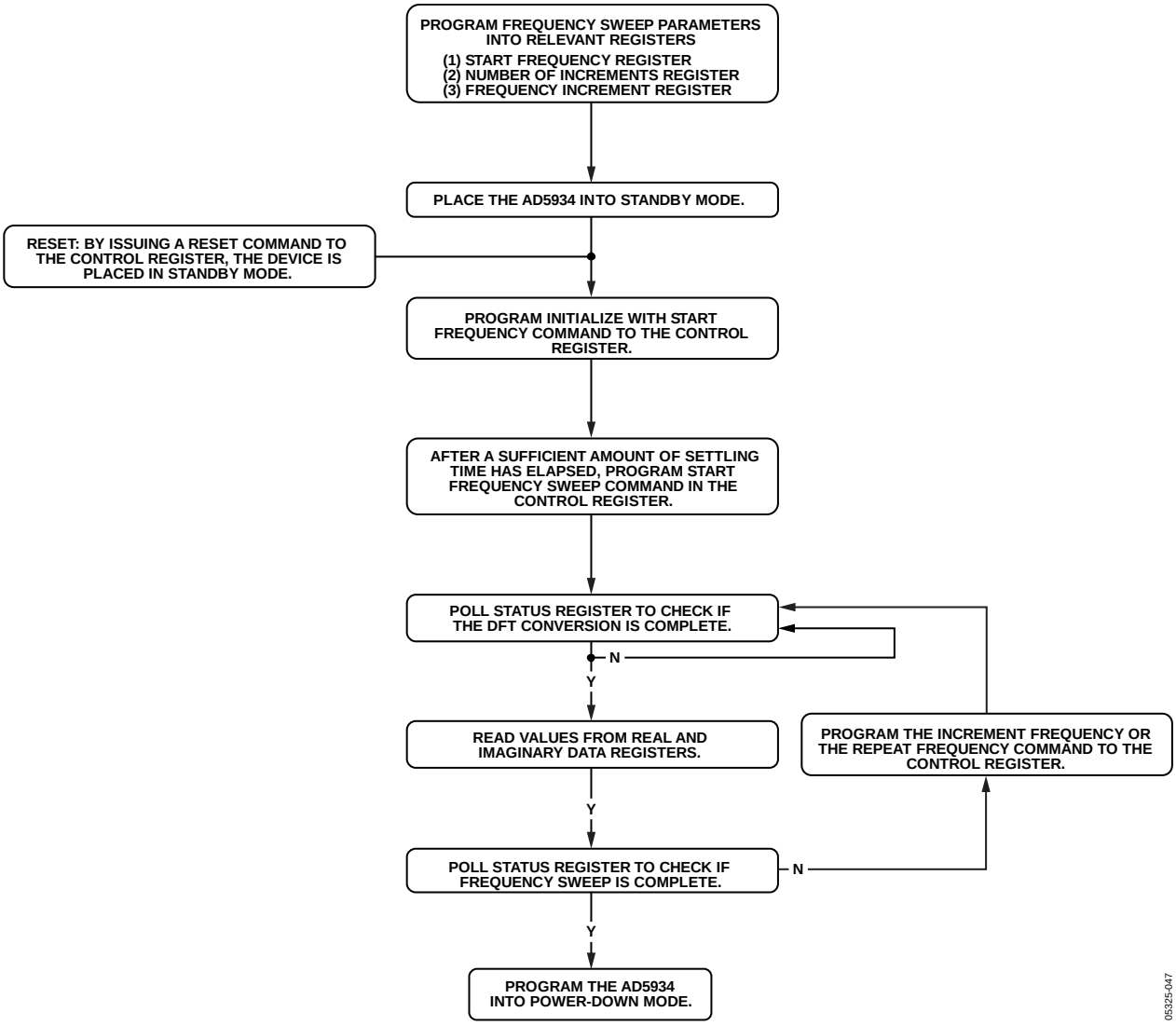


Figure 24. Frequency Sweep Flowchart

REGISTER MAP

Table 7.

Register Name	Register Address	Bits	Function
Control	0x80	D15 to D8	Read/write
	0x81	D7 to D0	Read/write
Start Frequency	0x82	D23 to D16	Read/write
	0x83	D15 to D8	Read/write
	0x84	D7 to D0	Read/write
Frequency Increment	0x85	D23 to D16	Read/write
	0x86	D15 to D8	Read/write
	0x87	D7 to D0	Read/write
Number of Increments	0x88	D15 to D8	Read/write
	0x89	D7 to D0	Read/write
Number of Settling Time Cycles	0x8A	D15 to D8	Read/write
	0x8B	D7 to D0	Read/write
Status	0x8F	D7 to D0	Read only
Real Data	0x94	D15 to D8	Read only
	0x95	D7 to D0	Read only
Imaginary Data	0x96	D15 to D8	Read only
	0x97	D7 to D0	Read only

CONTROL REGISTER (REGISTER ADDRESS 0x80, REGISTER ADDRESS 0x81)

The AD5934 contains a 16-bit control register (Register Address 0x80 and Register Address 0x81) that sets the control modes. The default value of the control register upon reset is as follows: D15 to D0 is reset to 0xA000 upon power-up.

The four MSBs of the control register are decoded to provide control functions, such as performing a frequency sweep, powering down the part, and controlling various other functions defined in the control register map.

The user can choose to write only to Register Address 0x80 and to not alter the contents of Register Address 0x81. Note that the control register should not be written to as part of a block write command. The control register also allows the user to program the excitation voltage and set the system clock. A reset command to the control register does not reset any programmed values associated with the sweep (that is, start frequency, number of increments, frequency increment). After a reset command, an initialize with start frequency command must be issued to the control register to restart the frequency sweep sequence (see Figure 24).

Table 8. D10 to D9 Control Register Map

D10	D9	Range No.	Output Voltage Range
0	0	1	2.0 V p-p typical
0	1	3	200 mV p-p typical
1	0	4	400 mV p-p typical
1	1	2	1.0 V p-p typical

Table 9. D11 and D8 to D0 Control Register Map

Bits	Description
D11	No operation
D8	PGA gain; 0 = ×5, 1 = ×1
D7	Reserved; set to 0
D6	Reserved; set to 0
D5	Reserved; set to 0
D4	Reset
D3	External system clock; set to 1
	Internal system clock; set to 0
D2	Reserved; set to 0
D1	Reserved; set to 0
D0	Reserved; set to 0

Table 10. D15 to D12 Control Register Map

D15	D14	D13	D12	Description
0	0	0	0	No operation
0	0	0	1	Initialize with start frequency
0	0	1	0	Start frequency sweep
0	0	1	1	Increment frequency
0	1	0	0	Repeat frequency
1	0	0	0	No operation
1	0	0	1	No operation
1	0	1	0	Power-down mode
1	0	1	1	Standby mode
1	1	0	0	No operation
1	1	0	1	No operation

Control Register Decode

Initialize with Start Frequency

This command enables the DDS to output the programmed start frequency for an indefinite time. Initially, it is used to excite the unknown impedance. When the output unknown impedance has settled after a time determined by the user, the user must initiate a start frequency sweep command to begin the frequency sweep.

Start Frequency Sweep

In this mode, the ADC starts measuring after the programmed number of settling time cycles has elapsed. The user has the ability to program an integer number of output frequency cycles (settling time cycles) to Register Address 0x8A and Register Address 0x8B before the commencement of the measurement at each frequency point (see Figure 24).

Increment Frequency

The increment frequency command is used to step to the next frequency point in the sweep. This usually happens after data from the previous step is transferred and verified by the DSP. When the AD5934 receives this command, it waits for the programmed number of settling time cycles before beginning the ADC conversion process.

Repeat Frequency

There is the facility to repeat the current frequency point measurement by issuing a repeat frequency command to the control register. This command allows users to average successive readings.

Power-Down Mode

The default state at power-up of the AD5934 is power-down mode. The control register contains the code 1010,0000,0000,0000 (0xA000). In this mode, both the output and input pins, VOUT and VIN, are connected internally to GND.

Standby Mode

This mode powers up the part for general operation. In standby mode, the VIN and VOUT pins are internally connected to GND.

Reset

A reset command allows the user to interrupt a sweep. The start frequency, number of increments, and frequency increment register contents are not overwritten. An initialize with start frequency command is required to restart the frequency sweep command sequence.

Output Voltage Range

The output voltage range allows the user to program the excitation voltage range at VOUT.

PGA Gain

The PGA gain allows the user to amplify the response signal into the ADC by a multiplication factor of ×5 or ×1.

START FREQUENCY REGISTER (REGISTER ADDRESS 0x82, REGISTER ADDRESS 0x83, REGISTER ADDRESS 0x84)

The start frequency register contains the 24-bit digital representation of the frequency from where the subsequent frequency sweep is initiated. For example, if the user requires the sweep to start from a frequency of 30 kHz using a 16.0 MHz clock, the user must program the value 0x3D to Register Address 0x82, the value 0x70 to Register Address 0x83, and the value 0xA3 to Register Address 0x84. Doing this ensures the output frequency starts at 30 kHz.

The start frequency code is

$$Start\ Frequency\ Code = \left(\frac{30\ \text{kHz}}{\left(\frac{16\ \text{MHz}}{16} \right)} \right) \times 2^{27} \equiv 0\text{x}3\text{D}70\text{A}3$$

The default value of the start frequency register upon reset is as follows: D23 to D0 are not reset at power-up. After the reset command, the contents of this register are not reset.

FREQUENCY INCREMENT REGISTER (REGISTER ADDRESS 0x85, REGISTER ADDRESS 0x86, REGISTER ADDRESS 0x87)

The frequency increment register contains a 24-bit representation of the frequency increment between consecutive frequency points along the sweep. For example, if the user requires an increment step of 30 Hz using a 16.0 MHz clock, the user must program the value 0x00 to Register Address 0x85, the value 0x0F to Register Address 0x86, and the value 0xBA to Register Address 0x87.

The formula for calculating the frequency increment is given by

$$Frequency\ Increment\ Code = \left(\frac{10\ \text{Hz}}{\left(\frac{16\ \text{MHz}}{16} \right)} \right) \times 2^{27} \equiv 0\text{x}00053\text{E}$$

The user programs the value 0x00 to Register Address 0x85, the value 0x05 to Register Address 0x86, and the value 0x3E to Register Address 0x87.

The default value of the frequency increment register upon reset is as follows: D23 to D0 are not reset at power-up. After the reset command, the contents of this register are not reset.

NUMBER OF INCREMENTS REGISTER (REGISTER ADDRESS 0x88, REGISTER ADDRESS 0x89)

The default value of the number of increments register upon reset is as follows: D8 to D0 are not reset at power-up. After a reset command, the contents of this register are not reset.

Table 11. Number of Increments Register

Reg Addr	Bits	Description	Function	Format
0x88	D15 to D9	Don't care	Read or write	Integer number stored in binary format
	D8	Number of increments	Read or write	
0x89	D7 to D0	Number of increments	Read or write	Integer number stored in binary format

This register determines the number of frequency points in the frequency sweep. The number of frequency points is represented by a 9-bit word, D8 to D0. D15 to D9 are don't care bits. This register in conjunction with the start frequency register and the frequency increment register determine the frequency sweep range for the sweep operation. The maximum number of increments that can be programmed is 511.

NUMBER OF SETTLING TIME CYCLES REGISTER (REGISTER ADDRESS 0x8A, REGISTER ADDRESS 0x8B)

The default value of the number of settling time cycles register upon reset is as follows: D10 to D0 are not reset at power-up. After a reset command, the contents of this register are not reset.

This register determines the number of output excitation cycles allowed to passthrough the unknown impedance after receipt of a start frequency sweep, increment frequency, or repeat frequency command, before the ADC is triggered to perform a conversion of the response signal. The number of settling time cycles register value determines the delay between a start frequency sweep/ increment frequency/repeat frequency command and the time an ADC conversion commences. The number of cycles is represented by a 9-bit word, D8 to D0. The value programmed into the number of settling time cycles register can be increased by a factor of 2 or 4, depending on the status of Bits D10 to D9. The five most significant bits, D15 to D11, are don't care bits. The maximum number of output cycles that can be programmed is 511 × 4 = 2044 cycles. For example, consider an excitation signal of 30 kHz, the maximum delay between the programming of this frequency and the time that this signal is first sampled by the ADC is ≈ 511 × 4 × 33.33 µs = 68.126 ms. The ADC takes 1024 samples, and the result is stored as real data and imaginary data in Register Address 0x94 to Register Address 0x97. The conversion process takes approximately 1 ms using a 16.777 MHz clock.

STATUS REGISTER (REGISTER ADDRESS 0x8F)

The status register is used to confirm that particular measurement tests have been successfully completed. Each of the bits from D7 to D0 indicate the status of a specific functionality of the AD5934.

Bit D0 and Bit D4 to Bit D7 are treated as don't care bits; these bits do not indicate the status of any measurement.

The status of Bit D1 indicates the status of a frequency point impedance measurement. This bit is set when the AD5934 completes the current frequency point impedance measurement. This bit indicates that there is valid real data and imaginary data in Register Address 0x94 to Register Address 0x97. This bit is reset on receipt of a start frequency sweep, increment frequency, repeat frequency, or reset command. This bit is also reset at power-up.

The status of Bit D2 indicates the status of the programmed frequency sweep. This bit is set when all programmed increments to the number of increments register are complete. This bit is reset at power-up and on receipt of a reset command.

Table 12. Status Register 0x8F

Control Word	Description
0000 0001	Reserved
0000 0010	Valid real/imaginary data
0000 0100	Frequency sweep complete
0000 1000	Reserved
0001 0000	Reserved
0010 0000	Reserved
0100 0000	Reserved
1000 0000	Reserved

Table 13. Number of Settling Times Cycles Register

Register Address	Bits	Description			Function	Format
0x8A	D15 to D11	Don't care			Read or write	Integer number stored in binary format
	D10 to D9	2-bit decode				
		D10	**D9**	**Description**		
		0	0	Default		
		0	1	No of cycles ×2		
		1	0	Reserved		
		1	1	No of cycles ×4		
	D8	MSB number of settling time cycles				
0x8B	D7 to D0	Number of settling time cycles			Read or write	Data

Valid Real/Imaginary Data

This bit is set when data processing for the current frequency point is finished, indicating real/imaginary data available for reading. The bit is reset when a start frequency sweep/increment frequency/repeat frequency DDS command is issued. In addition, this bit is reset to 0 when a reset command is issued to the control register.

Frequency Sweep Complete

This bit is set when data processing for the last frequency point in the sweep is complete. This bit is reset when a start frequency sweep command is issued to the control register. This bit is also reset when a reset command is issued to the control register.

REAL AND IMAGINARY DATA REGISTERS (16 BITS—REGISTER ADDRESS 0x94, REGISTER ADDRESS 0x95, REGISTER ADDRESS 0x96, REGISTER ADDRESS 0x97)

These registers contain a digital representation of the real and imaginary components of the impedance measured for the current frequency point. The values are stored in 16-bit, twos complement format. To convert this number to an actual impedance value, the magnitude, $\sqrt{(Real^2 + Imaginary^2)}$, must be multiplied by an admittance/code number (called a gain factor) to give the admittance and the result inverted to give the impedance. The gain factor varies for each ac excitation voltage/gain combination.

The default value upon reset: these registers are not reset at power-up or on receipt of a reset command. Note that the data in these registers is only valid if Bit D1 in the status register is set, indicating that the processing at the current frequency point is complete.

SERIAL BUS INTERFACE

Control of the AD5934 is carried out via the I²C-compliant serial interface protocol. The AD5934 is connected to this bus as a slave device under the control of a master device. The AD5934 has a 7-bit serial bus slave address. When the device is powered up, it has a default serial bus address, 0001101 (0x0D).

GENERAL I²C TIMING

Figure 25 shows the timing diagram for general read and write operations using the I²C-compliant interface.

The master initiates data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line (SDA) while the serial clock line (SCL) remains high. This indicates that a data stream follows. The slave responds to the start condition and shifts in the next 8 bits, consisting of a 7-bit slave address (MSB first) and an R/W bit, which determines the direction of the data transfer, that is, whether data is written to or read from the slave device (0 = write, 1 = read).

The slave responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit, and holding it low during the high period of this clock pulse. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is 0, the master writes to the slave device. If the R/W bit is 1, the master reads from the slave device.

Data is sent over the serial bus in sequences of nine clock pulses, 8 bits of data followed by an acknowledge bit, which can be from the master or slave device. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period because a low-to-high transition when the clock is high can be interpreted as a stop signal. If the operation is a write operation, the first data byte after the slave address is a command byte. This tells the slave device what to expect next. It may be an instruction telling the slave device to expect a block write, or it may be a register address that tells the slave where subsequent data is to be written. Because data can flow in only one direction as defined by the R/W bit, it is not possible to send a command to a slave device during a read operation. Before performing a read operation, it is sometimes necessary to perform a write operation to tell the slave what sort of read operation to expect and/or the address from which data is to be read.

When all data bytes are read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device releases the SDA line during the low period before the ninth clock pulse, but the slave device does not pull it low. This is known as a no acknowledge. The master then takes the data line low during the low period before the 10th clock pulse, and then high during the 10th clock pulse to assert a stop condition.

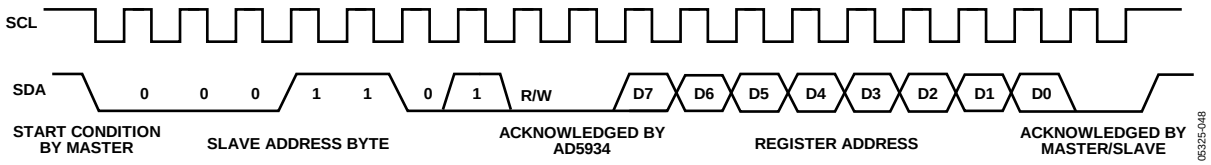


Figure 25. Timing Diagram

WRITING/READING TO THE AD5934

The I²C interface specification defines several different protocols for different types of read and write operations. This section describes the protocols used in the AD5934. The figures in this section use the abbreviations shown in Table 14.

Table 14. I²C Abbreviation Table

Abbreviation	Condition
S	Start
P	Stop
R	Read
W	Write
A	Acknowledge
$\overline{A}$	No acknowledge write byte/command byte

User Command Codes

The command codes in Table 15 are used for reading/writing to the interface. They are explained in detail in this section but are grouped within Table 15 for easy reference.

Table 15. Command Codes

Command Code	Code Name	Code Description
1010 0000	Block Write	This command is used when writing multiple bytes to the RAM; see the Block Write section.
1010 0001	Block Read	This command is used when reading multiple bytes from RAM/memory; see the Block Read section.
1011 0000	Address Pointer	This command enables the user to set the address pointer to any location in the memory; the data contains the address of the register to which the pointer should be pointing.

Write Byte/Command Byte

In this operation, the master device sends a byte of data to the slave device. The write byte can either be a data byte write to a Register Address or it can be a command operation. To write data to a register, the command sequence is as follows (see Figure 26):

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a register address.
5. The slave asserts an acknowledge on SDA.
6. The master sends a data byte.
7. The slave asserts an acknowledge on SDA.
8. The master asserts a stop condition on SDA to end the transaction.

Figure 26. Writing Register Data to Register Address

In the AD5934, the write byte protocol is also used to set a pointer to a register address (see Figure 27). This protocol is used for a subsequent single-byte read from the same address, block read, or block write starting at that address.

To set a register pointer, the following sequence is applied:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a pointer command code (see Table 15, an address pointer = 1011 0000).
5. The slave asserts an acknowledge on SDA.
6. The master sends a data byte (a register address to where the pointer is to point).
7. The slave asserts an acknowledge on SDA.
8. The master asserts a stop condition on SDA to end the transaction.

Figure 27. Setting Address Pointer to Register Address

BLOCK WRITE

In this operation, the master device writes a block of data to a slave device (see Figure 28). The start address for a block write must previously have been set. In the case of the AD5934, this is done by setting a pointer to set the register address.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends an 8-bit command code (1010 0000) that tells the slave device to expect a block write.
5. The slave asserts an acknowledge on SDA.
6. The master sends a data byte that tells the slave device the number of data bytes to be sent to it.
7. The slave asserts an acknowledge on SDA.
8. The master sends the data bytes.
9. The slave asserts an acknowledge on SDA after each data byte.
10. The master asserts a stop condition on SDA to end the transaction.

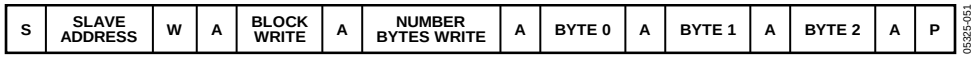


Figure 28. Writing a Block Write

READ OPERATIONS

The AD5934 uses two I²C read protocols: the receive byte and the block read.

Receive Byte

In the AD5934, the receive byte protocol is used to read a single byte of data from a register address whose address has previously been set by setting the address pointer.

In this operation, the master device receives a single byte from a slave device as follows (see Figure 29):

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master receives a data byte.
5. The master asserts a no acknowledge on SDA (the slave needs to check that master has received data).
6. The master asserts a stop condition on SDA and the transaction ends.

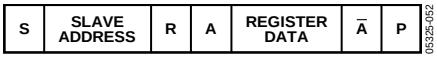


Figure 29. Reading Register Data

Block Read

In this operation, the master device reads a block of data from a slave device (see Figure 30). The start address for a block read must previously have been set by setting the address pointer.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a command code (1010 0001) that tells the slave device to expect a block read.
5. The slave asserts an acknowledge on SDA.
6. The master sends a byte-count data byte that tells the slave how many data bytes to expect.
7. The slave asserts an acknowledge on SDA.
8. The master asserts a repeat start condition on SDA. This is required to set the read bit high.
9. The master sends the 7-bit slave address followed by the read bit (high).
10. The slave asserts an acknowledge on SDA.
11. The master receives the data bytes.
12. The master asserts an acknowledge on SDA after each data byte.
13. A no acknowledge is generated after the last byte to signal the end of the read.
14. The master asserts a stop condition on SDA to end the transaction.

Figure 30. Performing a Block Read

TYPICAL APPLICATIONS

MEASURING SMALL IMPEDANCES

The AD5934 is capable of measuring impedance values up to 10 MΩ if the system gain settings are chosen correctly for the impedance subrange of interest.

If the user places a small impedance value (≤500 Ω over the sweep frequency of interest) between the VOUT and VIN pins, it results in an increase in signal current flowing through the impedance for a fixed excitation voltage in accordance with Ohm's law. The output stage of the transmit side amplifier available at the VOUT pin may not be able to provide the required increase in current through the impedance. To have a unity gain condition about the receive side I-V amplifier, the user needs to have a similar small value of feedback resistance for system calibration as outlined in the Gain Factor Setup Configuration section. The voltage presented at the VIN pin is hard biased at VDD/2 due to the virtual earth on the receive side I-V amplifier. The increased current sink/source requirement placed on the output of the receive side I-V amplifier may also cause the amplifier to operate outside of the linear region. This causes significant errors in subsequent impedance measurements.

The value of the output series resistance, R_{OUT}, (see Figure 31) at the VOUT pin must be taken into account when measuring small impedances ($Z_{UNKNOWN}$), specifically when the value of the output series resistance is comparable to the value of the impedance under test ($Z_{UNKNOWN}$). If the R_{OUT} value is unaccounted for in the system calibration (that is, the gain factor calculation) when measuring small impedances, there is an introduced error into any subsequent impedance measurement that takes place. The introduced error depends on the relative magnitude of the impedance being tested compared to the value of the output series resistance.

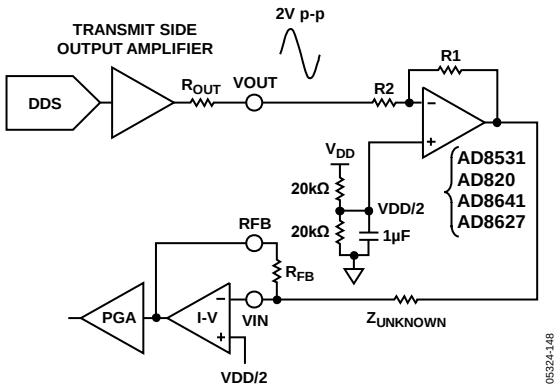


Figure 31. Additional External Amplifier Circuit for Measuring Small Impedances

The value of the output series resistance depends upon the selected output excitation range at VOUT and has a tolerance from device to device like all discrete resistors manufactured in a silicon fabrication process. Typical values of the output series resistance are outlined in Table 16.

Table 16. Output Series Resistance (R_{OUT}) vs. Excitation Range

Parameter	Value (Typ)	Output Series Resistance Value
Range 1	2 V p-p	200 Ω typical
Range 2	1 V p-p	2.4 kΩ typical
Range 3	0.4 V p-p	1.0 kΩ typical
Range 4	0.2 V p-p	600 Ω typical

Therefore, to accurately calibrate the AD5934 to measure small impedances, it is necessary to reduce the signal current by attenuating the excitation voltage sufficiently and also account for the R_{OUT} value and factor it into the gain factor calculation (see the Gain Factor Calculation section).

Measuring the R_{OUT} value during device characterization is achieved by selecting the appropriate output excitation range at VOUT and sinking and sourcing a known current at the pin (for example, ±2 mA) and measuring the change in dc voltage. The output series resistance can be calculated by measuring the inverse of the slope (that is, 1/slope) of the resultant I-V plot.

A circuit that helps to minimize the effects of the issues previously outlined is shown in Figure 31. The aim of this circuit is to place the AD5934 system gain within its linear range when measuring small impedances by using an additional external amplifier circuit along the signal path. The external amplifier attenuates the peak-to-peak excitation voltage at VOUT by a suitable choice of resistors (R1 and R2), thereby reducing the signal current flowing through the impedance and minimizing the effect of the output series resistance in the impedance calculations.

In the circuit shown in Figure 31, $Z_{UNKNOWN}$ recognizes the output series resistance of the external amplifier which is typically much less than 1 Ω with feedback applied depending upon the op amp device used (for example, AD820, AD8641, AD8531) as well as the load current, bandwidth, and gain.

The key point is that the output impedance of the external amplifier in Figure 31 (which is also in series with $Z_{UNKNOWN}$) has a far less significant effect on gain factor calibration and subsequent impedance readings in comparison to connecting the small impedance directly to the VOUT pin (and directly in series with R_{OUT}). The external amplifier buffers the unknown impedance from the effects of R_{OUT} and introduces a smaller output impedance in series with $Z_{UNKNOWN}$.

For example, if the user measures $Z_{UNKNOWN}$ that is known to have a small impedance value within the range of 90 Ω to 110 Ω over the frequency range of 30 kHz to 32 kHz, the user may not be in a position to measure R_{OUT} directly in the factory/lab. Therefore, the user may choose to add on an extra amplifier circuit like that shown in Figure 31 to the signal path of the AD5934. The user must ensure that the chosen external amplifier has a sufficiently low output series resistance over the bandwidth of interest in comparison to the impedance range under test (for an op amp selection guide, see www.analog.com/opamps). Most amplifiers from Analog Devices have a curve of closed-loop output impedance vs. frequency at different amplifier gains to determine the output series impedance at the frequency of interest.

The system settings are as follows:

VDD = 3.3 V

VOUT = 2 V p-p

R2 = 20 kΩ

R1 = 4 kΩ

Gain setting resistor = 500 Ω

$Z_{UNKNOWN}$ = 100 Ω

PGA setting = ×1

To attenuate the excitation voltage at VOUT, choose a ratio of R1/R2. With the values of R1 = 4 kΩ and R2 = 20 kΩ, attenuate the signal by 1/5th of 2 V p-p = 400 mV. The maximum current flowing through the impedance is 400 mV/90 Ω = 4.4 mA.

The system is subsequently calibrated using the usual method with a midpoint impedance value of 100 Ω, a calibration resistor, and a feedback resistor at a midfrequency point in the sweep. The dynamic range of the input signal to the receive side of the AD5934 can be improved by increasing the value of the I-V gain resistor at the RFB pin. For example, increasing the I-V gain setting resistor at the RFB pin increases the peak-to-peak signal presented to the ADC input from 400 mV (RFB = 100 Ω) to 2 V p-p (RFB = 500 Ω).

The gain factor calculated is for a 100 Ω resistor connected between VOUT and VIN, assuming the output series resistance of the external amplifier is small enough to be ignored.

When biasing the circuit shown in Figure 31, note that the receive side of the AD5934 is hard-biased about VDD/2 by design. Therefore, to prevent the output of the external amplifier (attenuated AD5934 Range 1 excitation signal) from saturating the receive side amplifiers of the AD5934, a voltage equal to VDD/2 must be applied to the noninverting terminal of the external amplifier.

BIOMEDICAL: NONINVASIVE BLOOD IMPEDANCE MEASUREMENT

When a known strain of a virus is added to a blood sample that already contains a virus, a chemical reaction takes place whereby the impedance of the blood under certain conditions changes. By characterizing this effect across different frequencies, it is possible to detect a specific strain of virus. For example, a strain of the disease exhibits a certain characteristic impedance at one frequency but not at another, resulting in the need to sweep different frequencies to check for different viruses. The AD5934, with its 27-bit phase accumulator, allows for subhertz frequency tuning.

The AD5934 can be used to inject a stimulus signal through the blood sample via a probe. The response signal is analyzed and the effective impedance of the blood is tabulated. The AD5934 is ideal for this application because it allows the user to tune to the specific frequency required for each test.

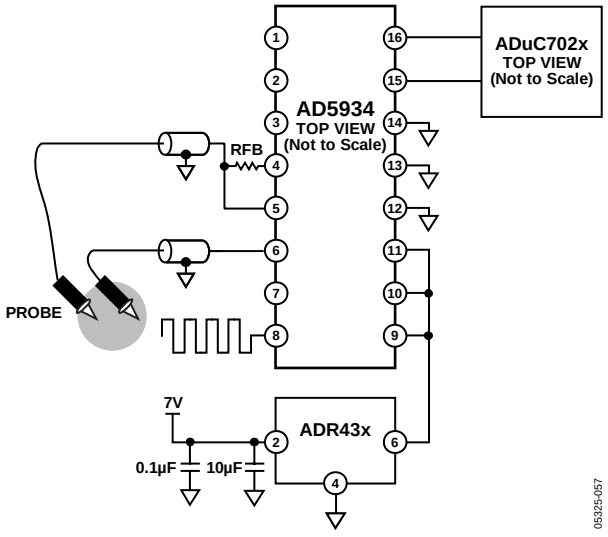


Figure 32. Measuring a Blood Sample for a Strain of Virus

SENSOR/COMPLEX IMPEDANCE MEASUREMENT

The operational principle of a capacitive proximity sensor is based on the change of a capacitance in a RLC resonant circuit. This leads to changes in the resonant frequency of the RLC circuit, which can be evaluated as shown Figure 33.

It is first required to tune the RLC circuit to the area of resonance. At the resonant frequency, the impedance of the RLC circuit is at a maximum. Therefore, a programmable frequency sweep and tuning capability is required, which is provided by the AD5934.

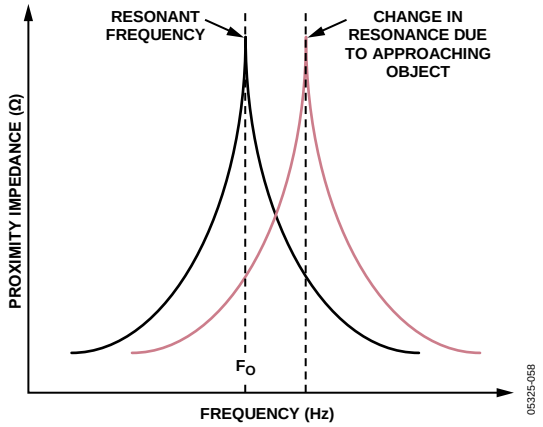


Figure 33. Detecting a Change in Resonant Frequency

An example of the use of this type of sensor is for a train proximity measurement system. The magnetic fields of the train approaching on the track change the resonant frequency to an extent that can be characterized. This information can be sent back to a mainframe system to show the train location on the network.

Another application for the AD5934 is in parked vehicle detection. The AD5934 is placed in an embedded unit connected to a coil of wire underneath the parking location. The AD5934 outputs a single frequency within the 80 kHz to 100 kHz frequency range, depending upon the wire composition. The wire can be modeled as a resonant circuit. The coil is calibrated with a known impedance value and at a known frequency. The impedance of the loop is monitored constantly. If a car is parked over the coil, the impedance of the coil changes and the AD5934 detects the presence of the car.

ELECTRO-IMPEDANCE SPECTROSCOPY

The AD5934 has found use in the area of corrosion monitoring. Corrosion in a metal, such as aluminum, which is used in air craft and ships, requires continuous assessment because the metal is exposed to a wide variety of conditions, such as temperature and moisture. The AD5934 offers an accurate and compact solution for this type of measurement compared to the large and expensive existing units on the market.

Mathematically the corrosion of a metal is modeled using a RC network that consists of a resistance, R_S, in series with a parallel resistor and capacitor, R_P and C_P. A system metal would typically have values as follows: R_S is 10 Ω to 10 kΩ, R_P is 1 kΩ to 1 MΩ, and C_P is 5 μF to 70 μF.

The frequency range of interest when monitoring corrosion is 0.1 Hz to 100 kHz.

To ensure that the measurement itself does not introduce a corrosive effect, the metal needs to be excited with minimal voltage, typically in the 200 mV region, which the AD5934 is capable of outputting. A nearby processor or control unit, such as the ADuc702x, would log a single impedance sweep from 0.1 kHz to 100 kHz every 10 minutes and download the results back to a control unit. To achieve system accuracy from the 0.1 kHz to 1 kHz region, the system clock needs to be scaled down from the 16.776 MHz nominal clock frequency to 500 kHz, typically. The clock scaling can be achieved digitally using an external direct digital synthesizer, such as the AD9834, as a programmable divider that supplies a clock signal to MCLK and that can be controlled digitally by the nearby microprocessor.

LAYOUT AND CONFIGURATION

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, carefully consider the power supply and ground return layout on the board. The printed circuit board (PCB) containing the AD5934 should have separate analog and digital sections, each having its own area of the board. If the AD5934 is in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5934.

The power supply to the AD5934 should be bypassed with 10 μF and 0.1 μF capacitors. The capacitors should be physically as close as possible to the device, with the 0.1 μF capacitor ideally right up against the device. The 10 μF capacitors are the tantalum bead type. It is important that the 0.1 μF capacitor has low effective series resistance (ESR) and effective series inductance (ESI); common ceramic types of capacitors are suitable. The 0.1 μF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feed-through effects on the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

OUTLINE DIMENSIONS

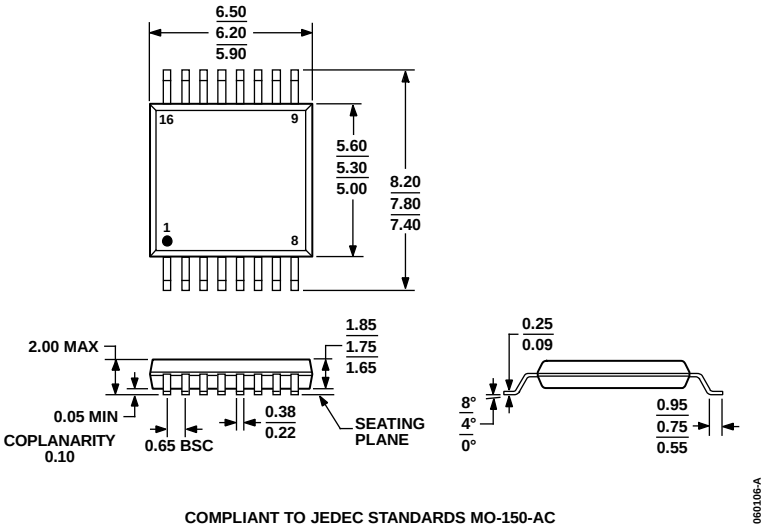


Figure 34. 16-Lead Shrink Small Outline Package [SSOP]
(RS-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD5934YRSZ	−40°C to +125°C	16-Lead Shrink Small Outline Package (SSOP)	RS-16
AD5934YRSZ-REEL7	−40°C to +125°C	16-Lead Shrink Small Outline Package (SSOP)	RS-16

[1] Z = RoHS Compliant Part.

NOTES

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

D05325-0-7/12(C)