VI BRICK® AC Front End

FE175D480C033FP-00

Size:
3.75 x 1.91 x 0.38 in
95,3 x 48,6 x 9,55 mm

Complete AC-DC PCB-mounted solution

Features

- Complete AC-DC PCB-mounted solution
- Active Power Factor Correction (PFC)
- Rectification
- Filtering
- Transient protection
- Low profile package, 9.55mm height above board
- Power density: 121 W/in^3, 330 W in 7.2 in^2 footprint
- Consistent high efficiency over world-wide AC mains (85 – 264 Vac)
- Secondary-side energy storage
- SELV 48 V Output
  - Efficient power distribution to POL converters
- 3,000 Vac /4,242 Vdc isolation
- PFC (THD) exceeds EN61000-3-2 requirements
- Conducted emissions EN55022, Class B (with a few external components)
- Surge immunity EN61000-4-5
- ZVS high frequency (MHz) switching
- Low profile, high-density filtering
- 100°C baseplate operation

Typical Applications

- LED - Lighting, display, signage
- Telecom (WiMAX, Power Amplifiers, Optical Switches)
- Automatic Test Equipment (ATE)
- High Efficiency Server Power
- Office Equipment (Printers, Copiers, Projectors)
- Industrial Equipment (Process Controllers, Material Handling, Factory Automation)

Product Overview

The VI BRICK® AC Front End is an AC-to-DC converter, operating from a universal AC input to generate an isolated and regulated 48 Vdc output with power factor correction. The module incorporates rectification, transient and surge suppression and AC to DC conversion to provide a complete AC to DC solution in a thin profile package. With its ZVS high frequency Adaptive Cell™ topology, the VI BRICK AC Front End module consistently delivers high efficiency across worldwide AC mains. Downstream DC-DC converters support secondary-side energy storage and efficient power distribution, providing superior power system performance and connectivity from the wall plug to the point-of-load.

Major Specifications

V_{IN}	85 – 264 V_{AC}
V_{OUT}	48 V_{DC} (isolated)
P_{OUT}	330 W

Nomenclature

Function		Input Voltage Designator			Package Size	Output Voltage Vout (V) (x10)			Temperature Grade	Output Power Pout (W) (÷10)			Baseplate	Pin Style		Revision	
F	E	1	7	5	D	4	8	0	C	0	3	3	F	P	–	0	0

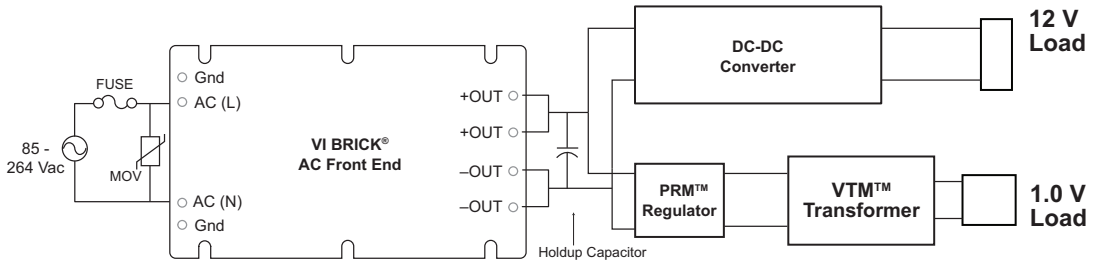
Universal (85 – 264 Vac)

Grade	Operating	Storage
C =	-20 to 100°C	-40 to 125°C
T =	-40 to 100°C	-40 to 125°C
M =	-55 to 100°C	-65 to 125°C

F = Slotted Flange

P = Through hole

Typical Application: Universal AC to 12 V and 1 V, total 300 W



Absolute Maximum Ratings

The ABSOLUTE MAXIMUM Ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to device. Electrical specifications do not apply when operating beyond rated operating conditions. Positive pin current represents current flowing out of the pin.

Parameter	Comments	Min	Max	Unit
Input voltage AC (L) to AC (N)	Continuous		275	V_{AC}
Input voltage AC (L) to AC (N)	1 ms	0	600	Vpk
RSV1 to –IN	Do not connect to this pin	-0.3	5.3	V_{DC}
EN to –IN	5 V tolerant 3.3 V logic	-0.3	5.3	V_{DC}
RSV3 to –IN	Do not connect to this pin	-0.3	5.3	V_{DC}
Output voltage (+Out to -Out)		-0.5	57.0	V_{DC}
Output current		0.0	10.2	A
Temperature				
Operating junction	Worst case semiconductor	0	125	°C
Operating temperature	C-Grade; baseplate	-20	100	°C
	T-Grade; baseplate	-40	100	°C
	M-Grade; baseplate	-55	100	°C
Storage temperature	C-Grade	-40	125	°C
	T-Grade	-40	125	°C
	M-Grade	-65	125	°C
Dielectric Withstand				
Dielectric Withstand Input – Output		3000		V_{RMS}
Dielectric Withstand Input – Base		1500		V_{RMS}
Dielectric Withstand Output – Base		1500		V_{RMS}

Electrical Characteristics

Specifications apply over all line and load conditions, 50 Hz and 60 Hz line frequencies, T_C = 25°C, unless otherwise noted.
Boldface specifications apply over the temperature range of the specified Product Grade. C_{OUT} is 6800uF +/- 20% unless otherwise specified.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Input Specification						
Input voltage range, continuous operation	V_{IN}		**85**		**264**	V_{RMS}
Input voltage cell reconfiguration low-to-high threshold	V_{IN-CR+}			145	**148**	V_{RMS}
Input voltage cell reconfiguration high-to-low threshold	V_{IN-CR-}		**132**	135		V_{RMS}
Input current (peak)	I_{INRP}				12	A
Source line frequency range	f_{line}		47		63	Hz
Power factor	PF	Input power > 100 W		0.9		-
Input inductance, (external)	L_{IN}	Differential-mode inductance, common-mode inductance may be higher			1	mH
No Load Specification						
Input power – no load, maximum	P_{NL}	EN floating, see Figure 4		1.1	1.5	W
Input power – disabled, maximum	P_Q	EN pulled low, see Figure 5			1.6	W
Power Output Specification						
Output voltage set point	V_{OUT}	Vin = 230 Vrms, 10% Load	47.5	49	50.5	V
Output voltage, no load	V_{OUT-NL}	Over all operating steady state line conditions	**46**	51.5	**55**	V
Output voltage range (transient)	V_{OUT}	Non-faulting abnormal line and load transient conditions	**30**		**55**	V
Output power	P_{OUT}	See Figure 1, Safe Operating Area			**330**	W
Efficiency	η	V_{IN} = 230 V, full load	91		94	%
		85 V < V_{IN} < 264 V, full load, see Figure 2	**88.5**			%
		85 V < V_{IN} < 264 V, 75% load	89			%
Output voltage ripple, switching frequency	$V_{OUT-PP-HF}$	Over all operating steady-state line and load conditions, 20 MHz BW, measured at C3, Figure 28.		100	**300**	mV
Output voltage ripple line frequency	$V_{OUT-PP-LF}$	Over all operating steady-state line and load conditions, 20 MHz BW		3.8	5	V
Output capacitance (external)	$C_{OUT-EXT}$		**6,000**		**12,000**	µF
Output turn-on delay	T_{ON}	From V_{IN} applied, EN floating		400	**1000**	ms
		From EN pin release, V_{IN} applied				
Start-up setpoint acquisition time	T_{SS}	Full load		400	500	ms
Cell reconfiguration response time	T_{CR}	Full load		5.5	11	ms
Voltage deviation (load transient)	$\%V_{OUT-TRANS}$	C_{OUT} = Max			8	%
Recovery time	T_{TRANS}			250	500	ms
Line regulation	$\%V_{OUT-LINE}$	Full load		0.5	1	%
Load regulation	$\%V_{OUT-LOAD}$	10% to 100% load		0.5	1	%
Output current (continuous)	I_{OUT}	See Figure 1, SOA			**6.9**	A

Electrical Characteristics (cont.)

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Output Specification (cont.)						
Output current (transient)	I_{OUT-PK}	20ms duration, max			**10.2**	A
Output switching cycle charge	Q_{TOT}				**13.5**	µC
Output inductance (parasitic)	$L_{OUT-PAR}$	Frequency @ 1 MHz		1		nH
Output capacitance (internal)	$C_{OUT-INT}$	Effective value at nominal output voltage		7		µF
Output capacitance (internal ESR)	R_{COUT}			0.5		mΩ
Powertrain Protections						
Input undervoltage turn-on	$V_{IN-UVLO+}$	See Timing Diagram		74	**83**	V_{RMS}
Input undervoltage turn-off	$V_{IN-UVLO-}$		**65**	71		V_{RMS}
Output overvoltage threshold	$V_{OUT-OVLO+}$	Instantaneous, latched shutdown	**55.3**	56.6	**59.0**	V
Upper start/restart temperature threshold (case)	$T_{CASE-OTP-}$		**100**			°C
Overtemperature shutdown threshold (junction)	T_{J-OTP+}		**130**			°C
Overtemperature shutdown threshold (case)	$T_{CASE-OTP+}$			**110**		°C
Undertemperature shutdown threshold (case)	$T_{CASE-UTP-}$	C Grade			**-25**	°C
Lower start / restart temperature threshold (case)	$T_{CASE-UTP+}$	C Grade			**-20**	°C
Overcurrent blanking time	T_{OC}	Based on line frequency	**400**	460	**550**	ms
Input overvoltage response time	T_{POVP}				**6**	µs
Input undervoltage response time	T_{UVLO}	Based on line frequency	**27**	39	**51**	ms
Output overvoltage response time	T_{SOVP}	Powertrain on	**60**	120	**180**	µs
Short circuit response time	T_{SC}	Powertrain on, operational state		60	**120**	µs
Fault retry delay time	T_{OFF}	See Timing Diagram		10		s
Output power limit	P_{PROT}		**330**			W

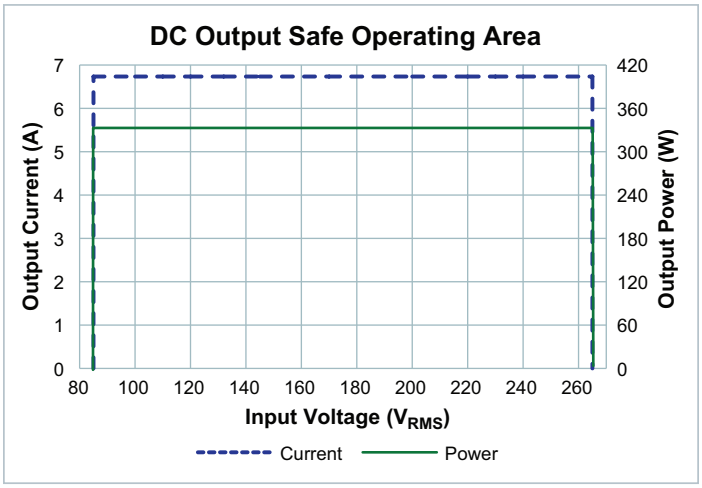


Figure 1 — DC output safe operating area

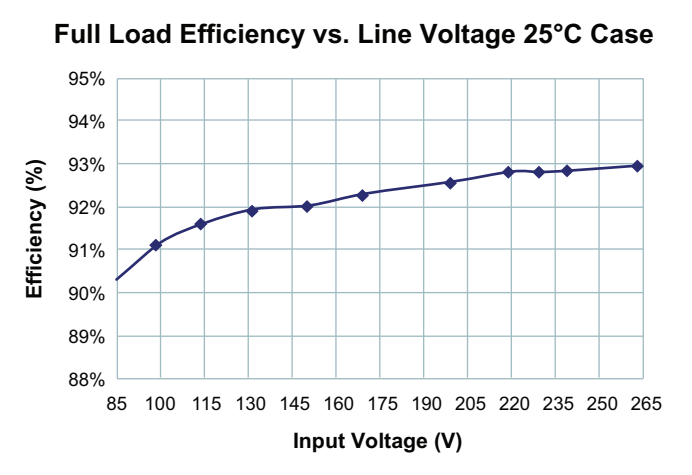


Figure 2 — Full load efficiency vs. line voltage

Signal Characteristics

Specifications apply over all line and load conditions, 50 Hz and 60 Hz line frequencies, T_C = 25°C, unless otherwise noted.
Boldface specifications apply over the temperature range of the specified Product Grade.

ENABLE : EN

- The EN pin enables and disables the VI BRICK® AC Front End; when held below 0.8 V the unit will be disabled.
- The EN pin can reset the VI BRICK AC Front End after a latching OVP event.
- The EN pin voltage is 3.3 V during normal operation.
- The EN pin is referenced to the –IN pin of the module.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Digital Input	Startup	EN enable threshold	V_{EN_EN}				**2.00**	V
	Standby	EN disable time	T_{EN_DIS}	From any point in line cycle		9	**16**	ms
		EN disable threshold	V_{EN_DIS}		**0.80**			V
		EN resistance to disable	R_{EN_EXT}	Max allowable resistance to -IN required to disable the module			**14**	kΩ

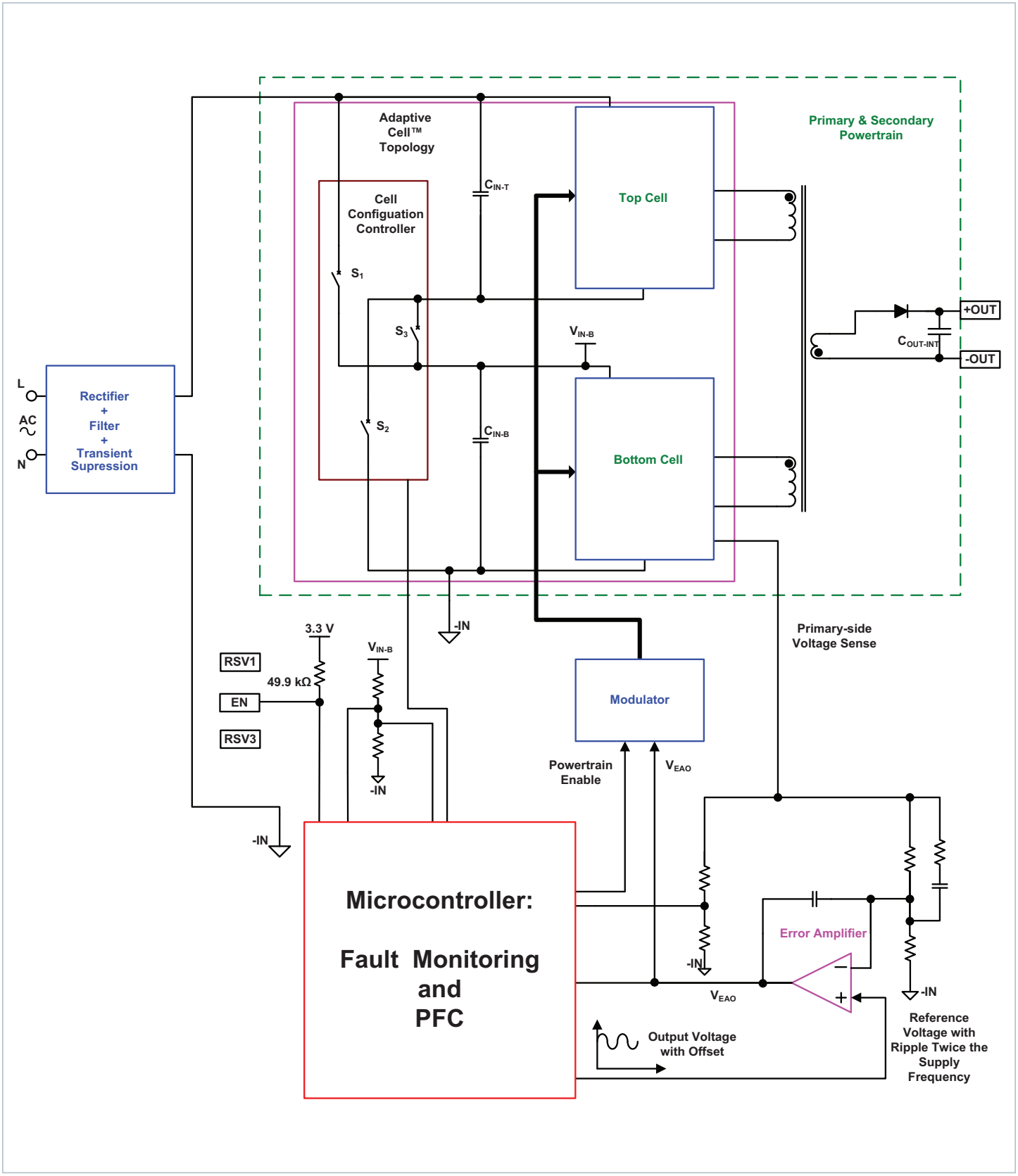
RESERVED : RSV1, RSV3

No connections should be made to these pins

-IN

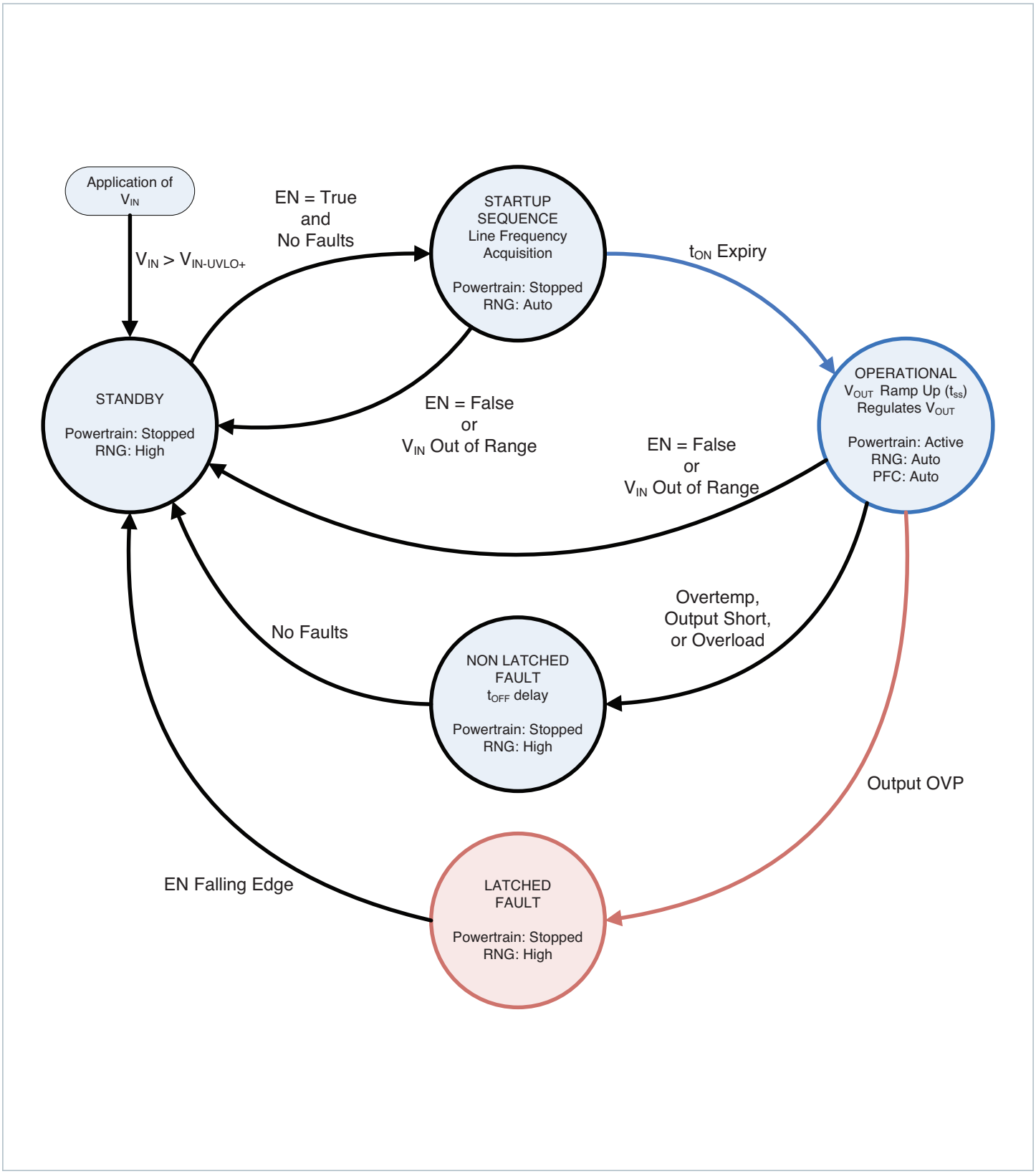
- **Warning:** -IN and N are not at the same potential and must not be connected together.
- The -IN pin is the signal reference ground for the EN pin
- The -IN pin also serves as an access point for the common mode bypass filter to comply with EN55022 Class B for Conducted Emissions.

Functional Block Diagram



High Level Functional State Diagram

Conditions that cause state transitions are shown along arrows. Sub-sequence activities listed inside the state bubbles.



Timing Diagrams

Module Inputs are shown in blue; Module Outputs are shown in brown.

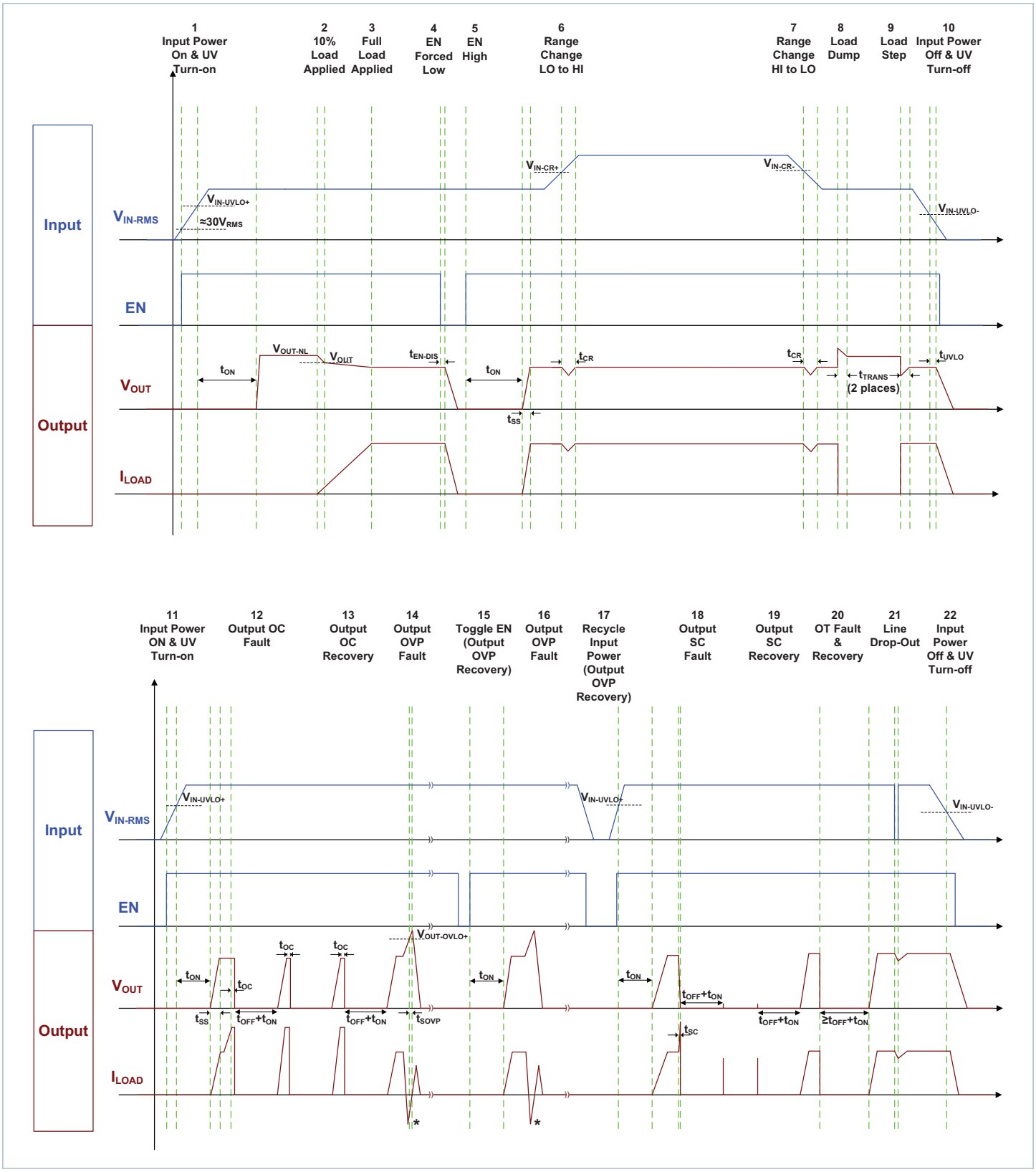


*Figure 3 — Timing diagram - * Negative current is externally forced and shown for the purpose of OVP protection scenario.*

Application Characteristics

The following figures present typical performance at T_C = 25°C, unless otherwise noted. See associated figures for general trend data.

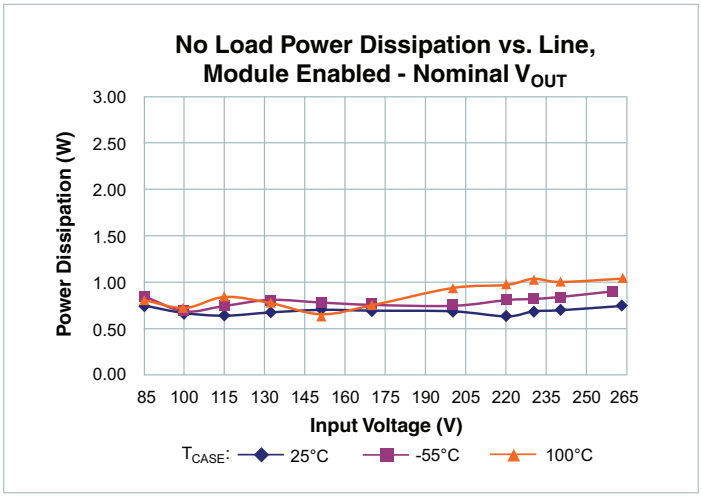


Figure 4 – *Typical no load power dissipation vs. V_{IN}, module enabled.*

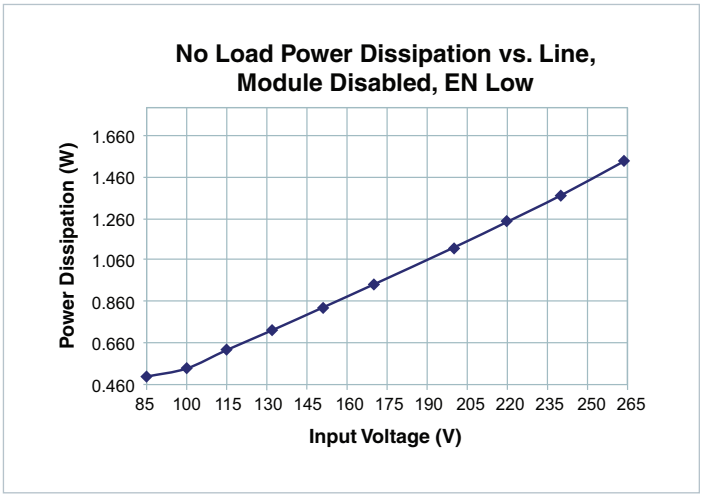


Figure 5 – *No load power dissipation trend vs. V_{IN}, module disabled.*

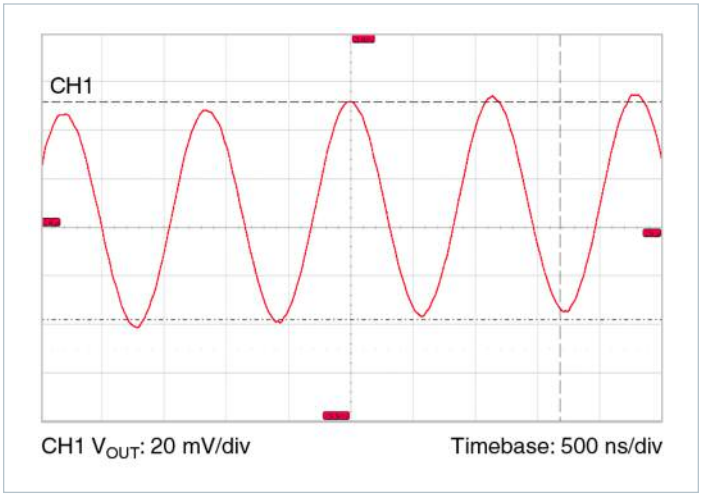


Figure 6 – *Typical switching frequency output voltage ripple waveform, T_{CASE} = 30°C, V_{IN} = 230 V, I_{OUT} = 6.9 A, no external ceramic capacitance.*

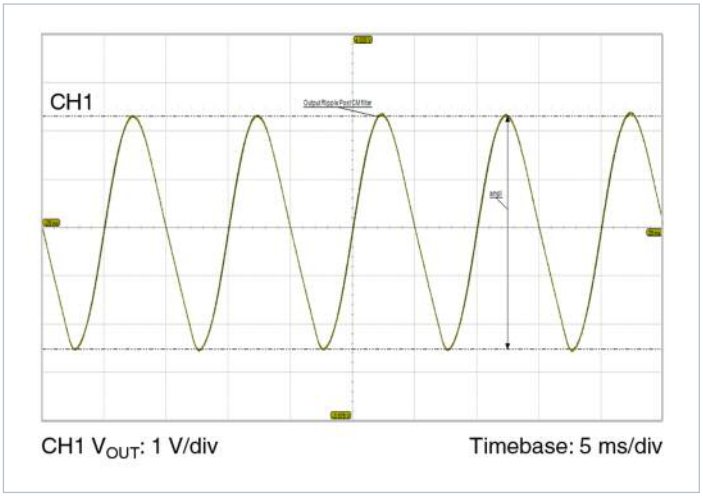


Figure 7 – *Typical line frequency output voltage ripple waveform, T_{CASE} = 30°C, V_{IN} = 230 V, I_{OUT} = 6.9 A, C_{OUT} = 6,800 µF. Measured at C3, Figure 28.*

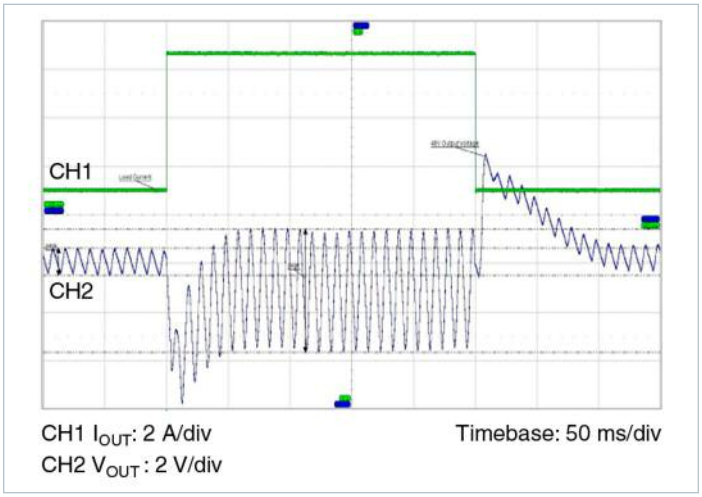


Figure 8 – *Typical output voltage transient response, T_{CASE} = 30°C, V_{IN} = 230 V, I_{OUT} = 6.9 A, C_{OUT} = 6,800 µF.*

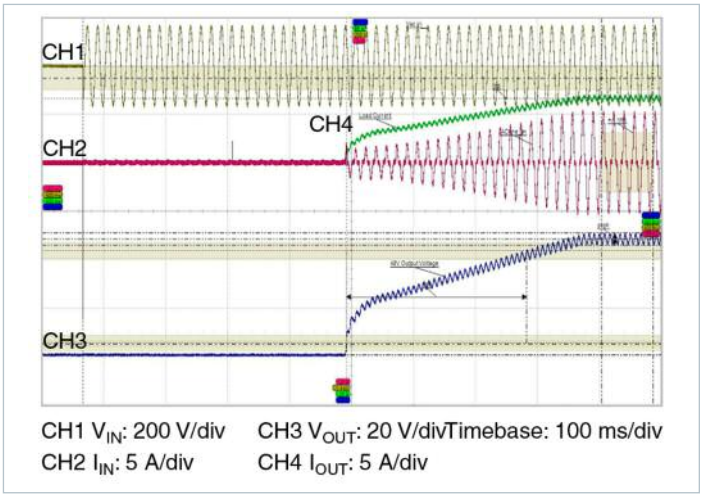


Figure 9 – *Typical startup waveform, application of V_{IN}, R_{LOAD} = 7.1 Ω, C_{OUT} = 6,800 µF.*

Application Characteristics (cont.)

The following figures present typical performance at T_C = 25°C, unless otherwise noted. See associated figures for general trend data.

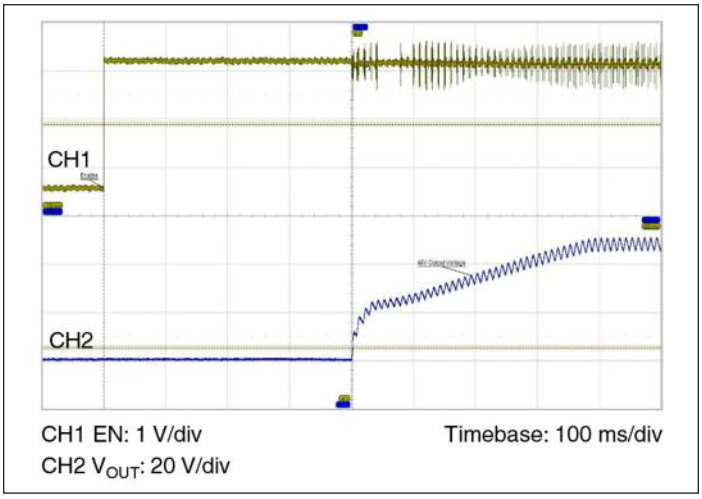


Figure 10 – *Typical startup waveform, EN pin release, V_{IN} = 230 V, R_{LOAD} = 7.1 Ω, C_{OUT} = 6,800 µF.*

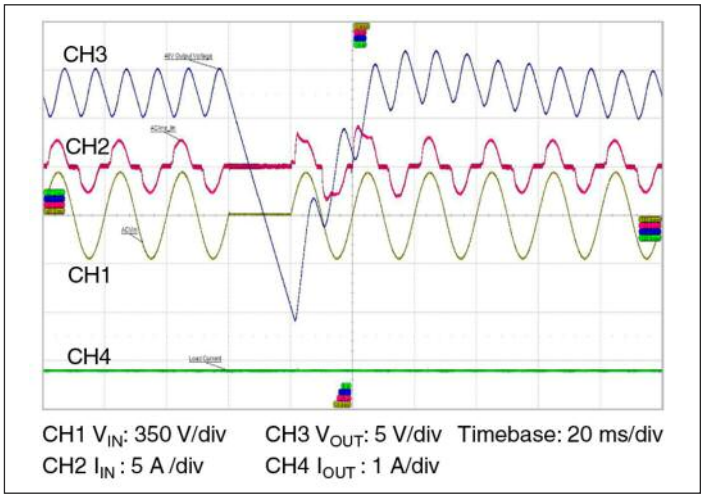


Figure 11 – *Line drop out, 50 Hz, 0° phase, P_{LOAD} = 330 W, C_{OUT} = 6,800 µF.*

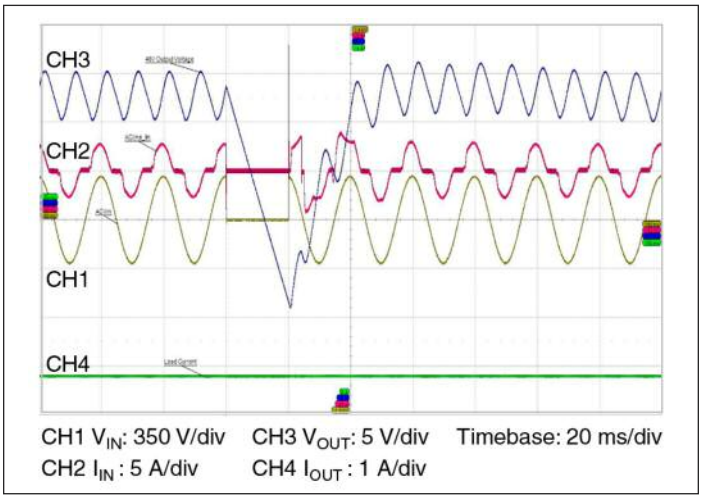


Figure 12 – *Line drop out, 50 Hz, 90° phase, V_{IN} = 230 V, P_{LOAD} = 330 W, C_{OUT} = 6,800 µF.*

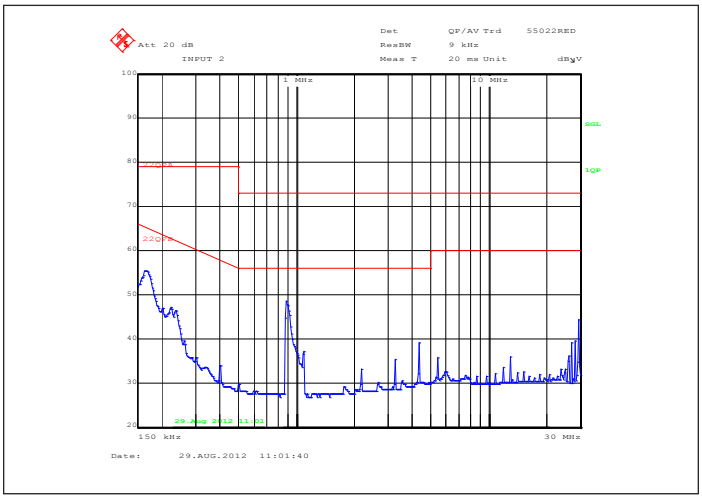


Figure 13 – *Typical EMI spectrum, Quasi-Peak Scan, 90% load, 230 V_{IN}, C_{OUT} = 6,800 µF. Test circuit - Figure 28.*

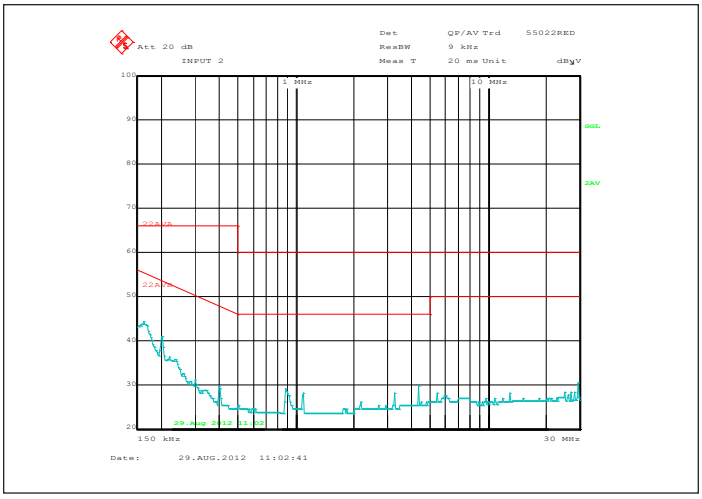


Figure 14 – *Typical EMI spectrum, Average Scan, 90% load, 230 V_{IN}, C_{OUT} = 6,800 µF. Test circuit - Figure 28.*

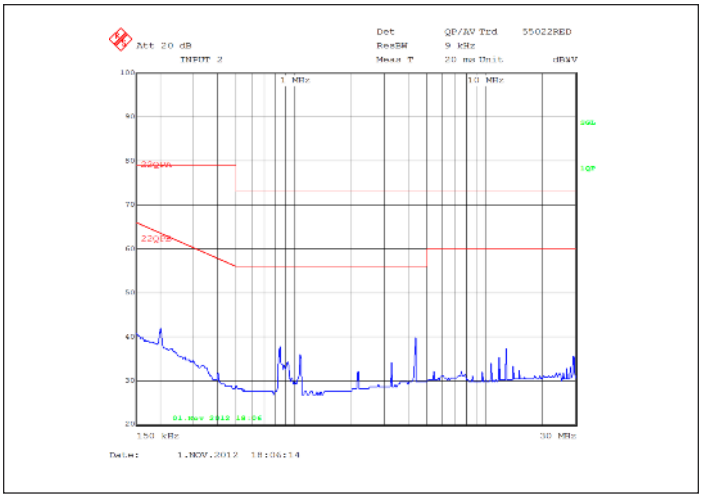


Figure 15 – *Typical EMI spectrum, Quasi-Peak Scan, 90% load, 115 V_{IN}, C_{OUT} = 6,800 µF. Test circuit - Figure 28.*

Application Characteristics (cont.)

The following figures present typical performance at T_C = 25°C, unless otherwise noted. See associated figures for general trend data.

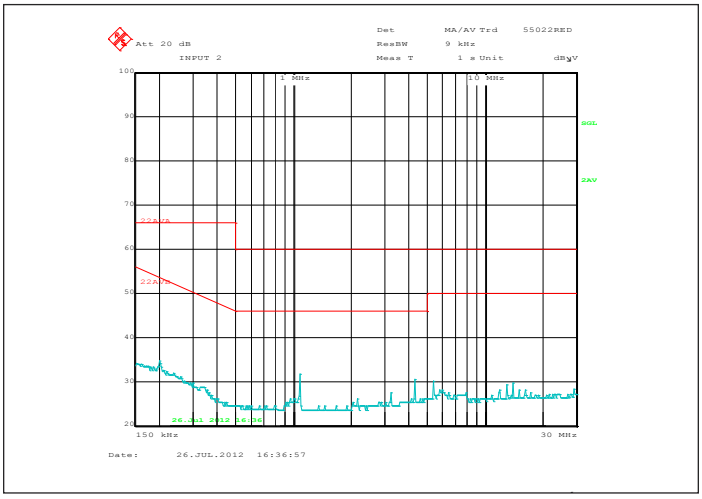


Figure 16 – *Typical EMI spectrum, Average Scan, 90% load, 115 V_{IN}, C_{OUT} = 6,800 µF. Test circuit - Figure 28.*

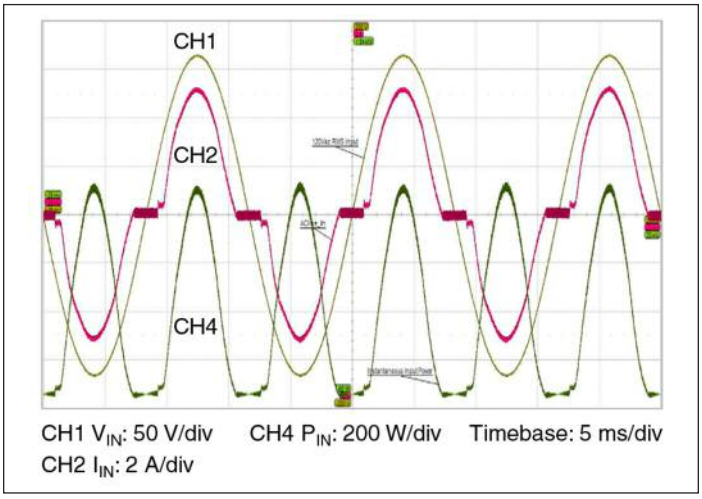


Figure 17 – *Typical line current waveform, 60 Hz, V_{IN} = 120 V, P_{LOAD} = 330 W. C_{OUT} = 6,800 µF.*

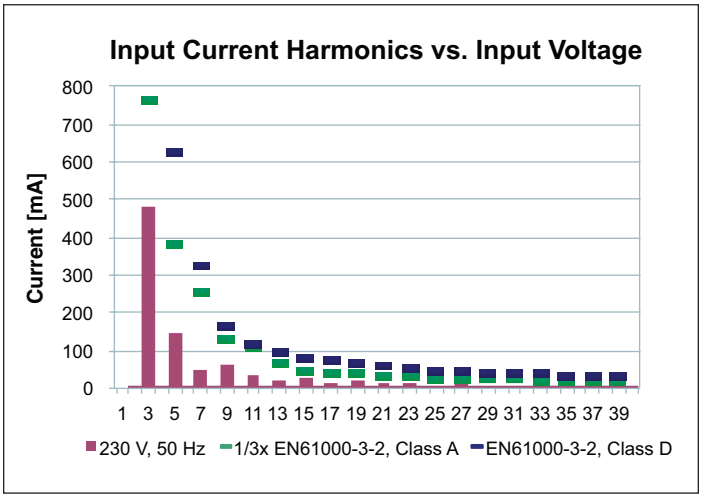


Figure 18 – *Typical input current harmonics, full load vs. V_{IN}.*

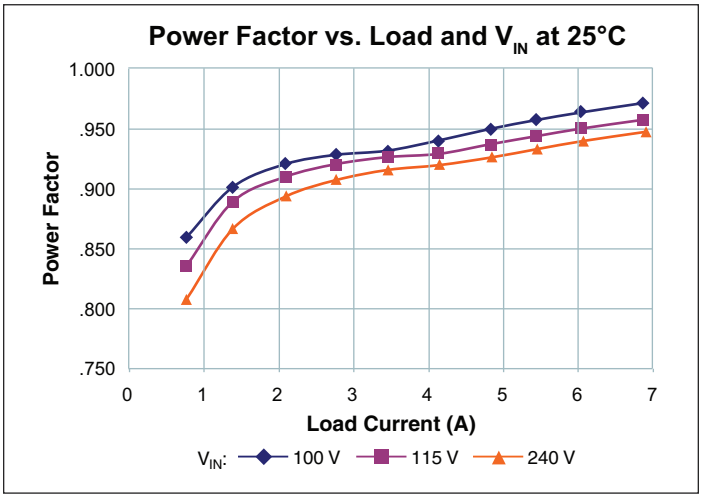


Figure 19 – *Typical power factor vs. V_{IN} and I_{OUT}.*

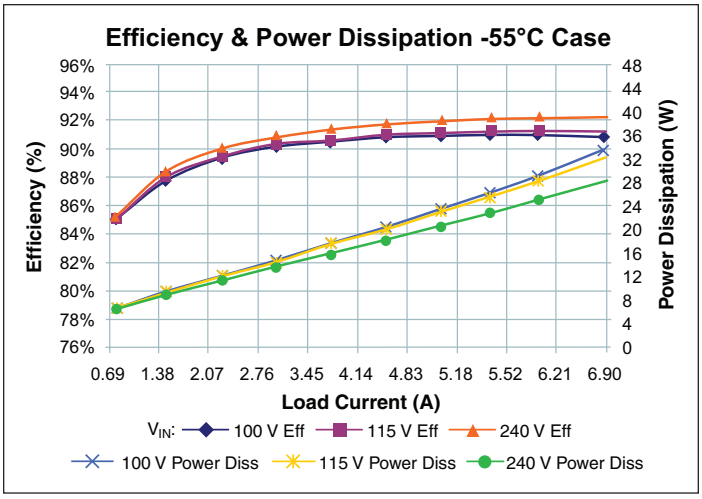


Figure 20 – *V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = -55°C.*

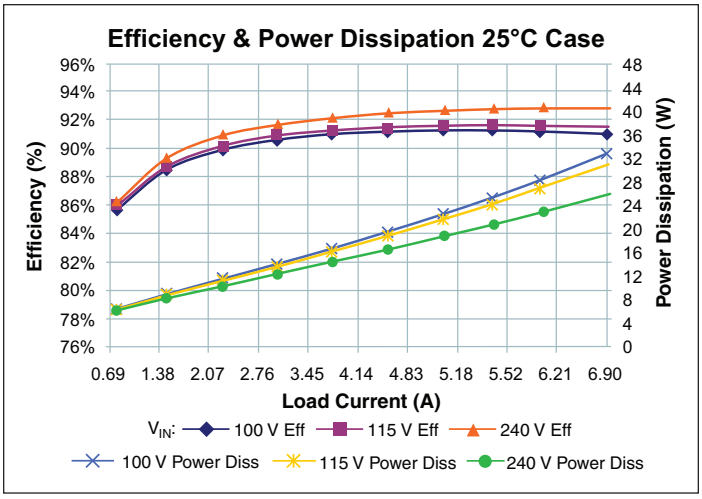


Figure 21 – *V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = 25°C.*

Application Characteristics (cont.)

The following figures present typical performance at T_C = 25ºC, unless otherwise noted. See associated figures for general trend data.

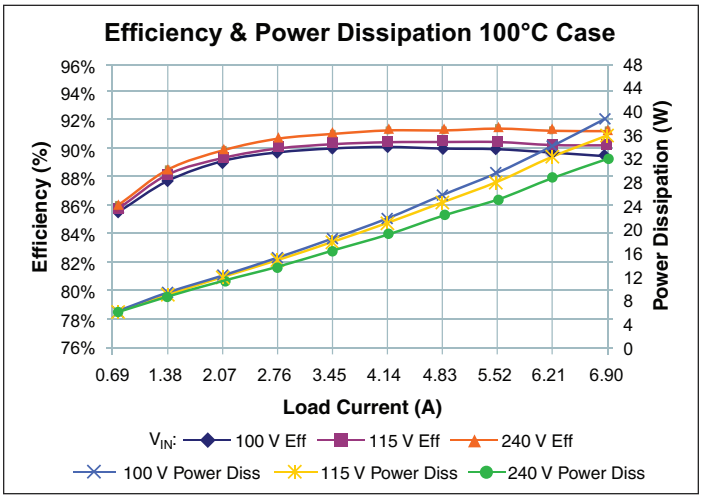


Figure 22 – *V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = 100ºC.*

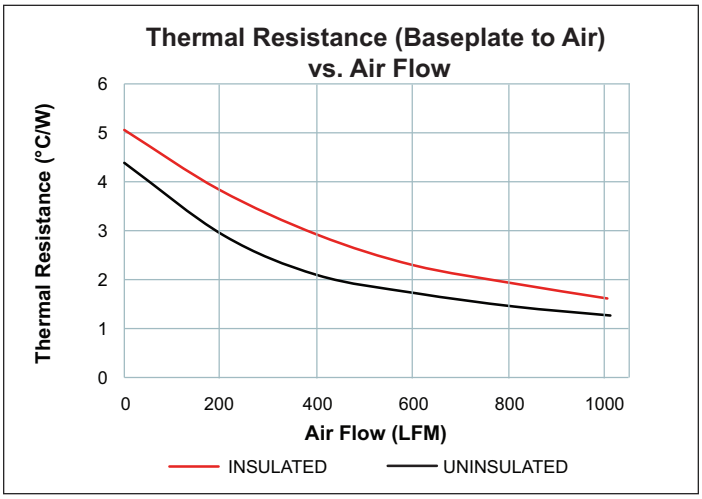


Figure 23 – *Baseplate to air thermal resistance Insulated – minimal thermal dissipation through pins to pcb; Uninsulated – thermal dissipation to typical pcb.*

General Characteristics

Specifications apply over all line and load conditions, 50 Hz and 60 Hz line frequencies, TC = 25°C, unless otherwise noted.
Boldface specifications apply over the temperature range of the specified Product Grade.

Attribute	Symbol	Conditions / Notes		Min	Typ	Max	Unit
Mechanical							
Length	L				95.3/[3.75]		mm/[in]
Width	W				48.6/[1.91]		mm/[in]
Height	H				9.55/[0.38]		mm/[in]
Volume	Vol				44.2/[2.69]		cm^3/[in^3]
Weight	W				111/[3.9]		g/[oz]
Pin material		C10200 copper, full hard					µin
Underplate		Nickel		100		150	
Pin finish		Pure matte tin, whisker resistant chemistry		200		300	
Thermal							
Operating baseplate (case) temperature	T_C	Any operating condition	C - Grade	-20		100	°C
			T - Grade	-40		100	°C
			M - Grade	-55		100	°C
Thermal resistance, baseplate-to-sink, flat greased surface					0.13		°C/W
Thermal resistance, baseplate-to-sink, thermal pad (PN 36967)					0.17		°C/W
Thermal capacity					84.5		Ws/°C
Thermal design		See Thermal Design on page 18					
Assembly							
ESD rating	ESD_{HBM}	Human Body Model, "JEDEC JESD 22-A114C.01"		1,000			V
	ESD_{MM}	Machine Model, "JEDEC JESD 22-A115B"		N/A			
	ESD_{CDM}	Charged Device Model, "JEDEC JESD 22-C101D"		200			
Soldering							
See application note		Soldering Methods and Procedure for Vicor Power Modules »					
Safety & Reliability							
Agency approvals/standards		cTÜVus (EN60950-1)					
		cURus (UL/CSA 60950-1)					
		CE, Low Voltage Directive 2006/95/EC					
		Touch Current measured in accordance with IEC 60990 using measuring network Figure 28			0.56	0.68	mA
EMI/EMC Compliance							
FCC Part 15, EN55022, CISPR22: 2006 + A1: 2007, Conducted Emissions		Class B Limits - with components connected as shown in Figure 28					
EN61000-3-2: 2009, Harmonic Current Emissions		Class A					
EN61000-3-3: 2005, Voltage Changes & Flicker		P_{ST}<1.0; P_{LT}<0.65; dc<3.3%; dmax<6%					

General Characteristics (cont.)

Specifications apply over all line and load conditions, 50 Hz and 60 Hz line frequencies, TC = 25°C, unless otherwise noted.
Boldface specifications apply over the temperature range of the specified Product Grade.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
EMI/EMC Compliance (cont.)						
EN61000-4-4: 2004, Electrical Fast Transients		Level 3, Performance Criteria A				
EN61000-4-5: 2006, Surge Immunity		Level 3, Immunity Criteria A, external TMOV required, limit input transient to 750 V				
EN61000-4-6: 2009, Conducted RF Immunity		Level 2, 130 dBµV (3.0 V_{RMS})				
EN61000-4-8: 1993 + A1 2001, Power Frequency H-Field 10A/m, continuous field		Level 3, Performance Criteria A				
EN61000-4-11: 2004, Voltage Dips & Interrupts		Class 2, Performance Criteria A Dips, Performance Criteria B Interrupts				

Product Outline Drawing and Recommended PCB Footprint

Module Outline

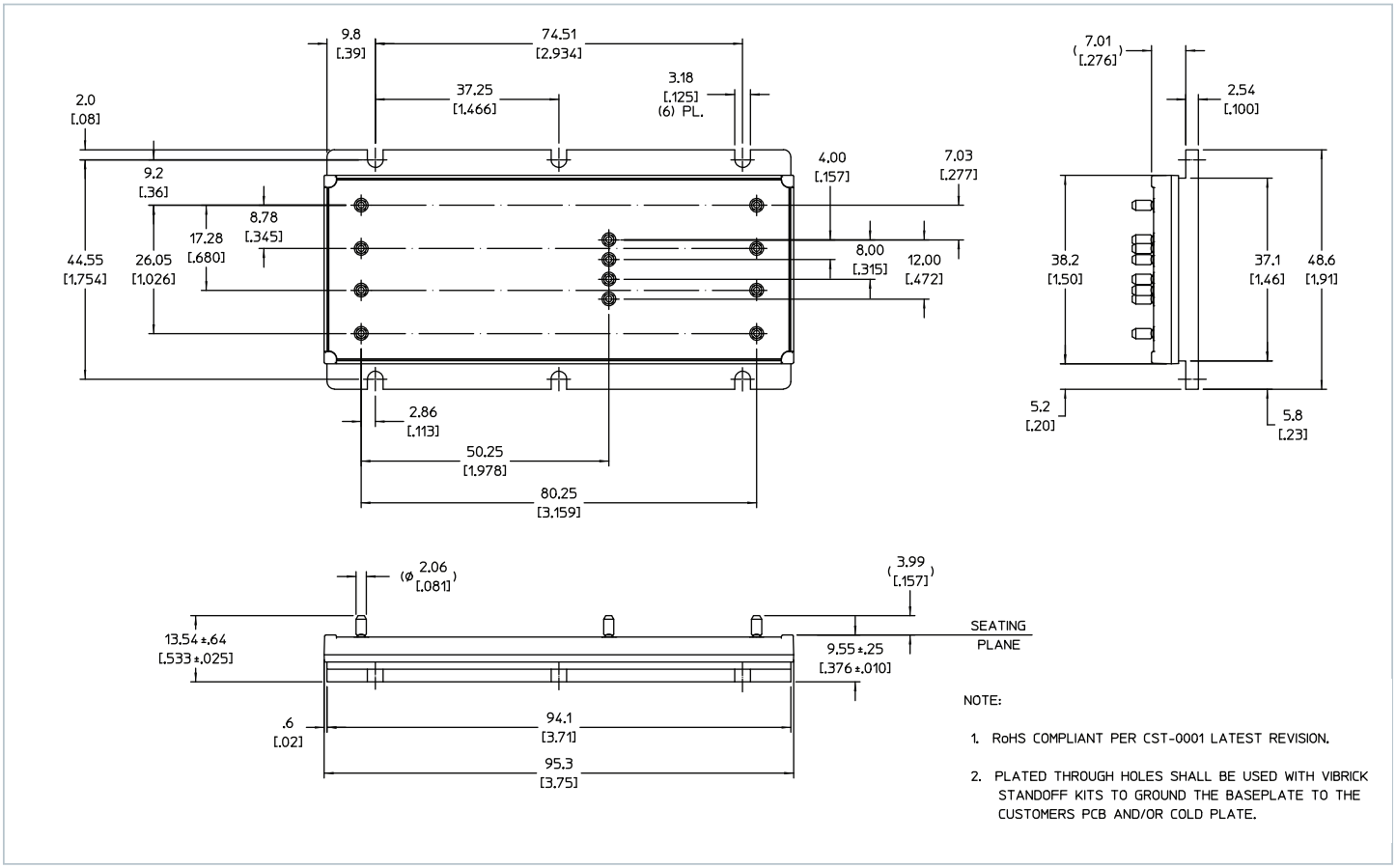
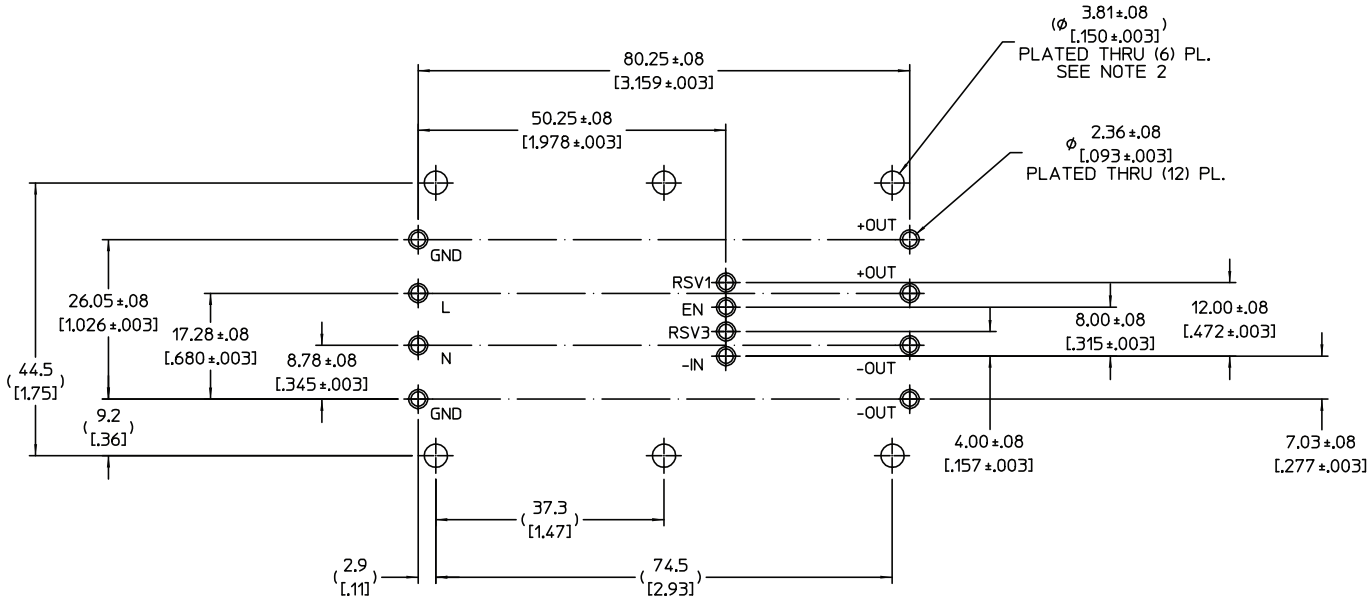


Figure 24 — *Product outline drawing;*
Product outline drawings are available in .pdf and .dxf formats.
3D mechanical models are available in .pdf and .step formats.
See http://www.vicorpower.com/cms/home/technical_resources/Mechanical_Drawings/Modules for more details.

Product Outline Drawing and Recommended PCB Footprint (cont.)

Mounting Specifications



RECOMMENDED PCB PATTERN
(COMPONENT SIDE SHOWN)

Figure 25— *Recommended PCB pattern;*
Product outline drawings are available in .pdf and .dxf formats.
3D mechanical models are available in .pdf and .step formats.
See http://www.vicorpower.com/cms/home/technical_resources/Mechanical_Drawings/Modules for more details.

Product Details and Design Guidelines

Building Blocks and System Designs

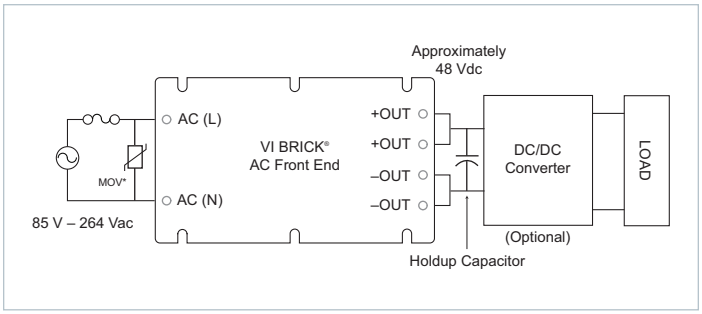


Figure 26 – *300 W Universal AC-to-DC Supply*

The VI BRICK® AC Front End is a high efficiency AC-to-DC converter, operating from a universal AC input to generate an isolated SELV 48 VDC output bus with power factor correction. It is the key component of an AC-to-DC power supply system such as the one shown in Figure 26 above.

The input to the VI BRICK AC Front End is a sinusoidal AC source with a power factor maintained by the module with harmonics conforming to IEC 61000-3-2. Internal filtering enables compliance with the standards relevant to the application (Surge, EMI, etc.). See EMI/EMC Compliance standards on page 13.

The module uses secondary-side energy storage (at the SELV 48 V bus) and optional PRM® regulators to maintain output hold up through line dropouts and brownouts. Downstream regulators also provide tighter voltage regulation, if required.

The FE175D480C033FP-00 is designed for standalone operation; however, it may be part of a system that is paralleled by downstream DC-DC converters. Contact Vicor Sales or refer to our website, www.vicorpower.com, regarding new models that can be paralleled directly for higher power applications.

Traditional PFC Topology

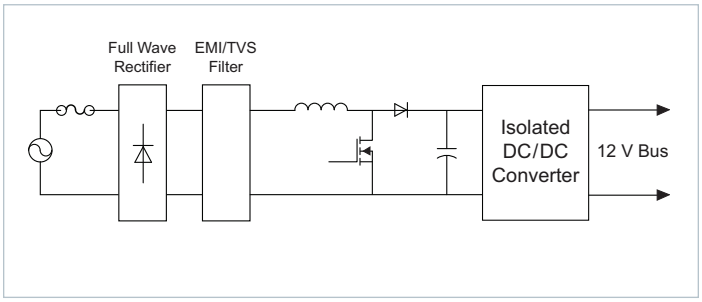


Figure 27 – *Traditional PFC AC-to-DC supply*

To cope with input voltages across worldwide AC mains (85 – 264 Vac), traditional AC-DC power supplies (Figure 27) use two power conversion stages: 1) a PFC boost stage to step up from a rectified input as low as 85 Vac to ~380 Vdc; and 2) a DC-DC down converter from 380 Vdc to a 12 V bus.
The efficiency of the boost stage and of traditional power supplies is significantly compromised operating from worldwide AC lines as low as 85 Vac.

Adaptive Cell™ Topology

With its single stage Adaptive Cell™ topology, the VI BRICK AC Front End enables consistently high efficiency conversion from worldwide AC mains to a 48 V bus and efficient secondary-side power distribution.

Power Factor Correction

The module provides power factor correction over worldwide AC mains. For most static loads, PFC approaches unity, see Figure 19. Load transients that approach the line frequency should be filtered or avoided as these may reduce PFC.

Input Fuse Selection

VI BRICK products are not internally fused in order to provide flexibility in configuring power systems. Input line fusing is recommended at system level, in order to provide thermal protection in case of catastrophic failure. The fuse shall be selected by closely matching system requirements with the following characteristics:

- Recommended fuse: 5 A, 216 Series Littelfuse
- Current rating
  (usually greater than the VI BRICK AC Front End maximum current)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Breaking capacity per application requirements
- Nominal melting I^2t

Fault Handling

Input Undervoltage (UV) Fault Protection

The VI BRICK AC Front End's input voltage (proportional to V_{IN-B} as shown on page 6) is monitored by the micro-controller to detect an input under voltage condition. When the input voltage is less than the $V_{IN-UVLO-}$, a fault is detected, the fault latch and reset logic disables the modulator, the modulator stops powertrain switching, and the output voltage of the unit falls. After a time t_{UVLO}, the unit shuts down. Faults lasting less than t_{UVLO} may not be detected. Such a fault does not go through an auto-restart cycle. Once the input voltage rises above $V_{IN-UVLO+}$, the unit recovers from the input UV fault, the powertrain resumes normal switching after a time t_{ON} and the output voltage of the unit reaches the set-point voltage within a time t_{SS}.

Overcurrent (OC) Fault Protection

The unit's output current, determined by V_{EAO}, V_{IN_B} and the primary-side sensed output voltage, (as shown on page 6) is monitored by the microcontroller to detect an output OC condition. If the output current exceeds its current limit, a fault is detected, the reset logic disables the modulator, the modulator stops powertrain switching, and the output voltage of the module falls after a time t_{OC}. As long as the fault persists, the module goes through an auto-restart cycle with off time equal to $t_{OFF} + t_{ON}$ and on time equal to t_{OC}. Faults shorter than a time t_{OC} may not be detected. Once the fault is cleared, the module follows its normal start up sequence after a time t_{OFF}.

Short Circuit (SC) Fault Protection

The microcontroller determines a short circuit on the output of the unit by measuring its primary sensed output voltage and EAO (as shown on page 6). Most commonly, a drop in the primary-sensed output voltage triggers a short circuit event. The module responds to a short circuit event within a time t_{SC}. The module then goes through an auto restart cycle, with an off time equal to $t_{OFF} + t_{ON}$ and an on time equal to t_{SC}, for as long as the short circuit fault condition persists. Once the fault is cleared, the unit follows its normal start up sequence after a time t_{OFF}. Faults shorter than a time t_{SC} may not be detected.

Product Details and Design Guidelines (cont.)

Temperature Fault Protection

The microcontroller monitors the temperature within the VI BRICK® AC Front End. If this temperature exceeds $T_{J\text{-}OTP+}$, an overtemperature fault is detected, the reset logic block disables the modulator, the modulator stops the powertrain switching and the output voltage of the VI BRICK AC Front End falls. Once the case temperature falls below $T_{CASE\text{-}OTP\text{-}}$, after a time greater than or equal to t_{OFF}, the converter recovers and undergoes a normal restart. For the C-grade version of the converter, this temperature is 75°C. Faults shorter than a time t_{OTP} may not be detected. If the temperature falls below $T_{CASE\text{-}UTP\text{-}}$, an undertemperature fault is detected, the reset logic disables the modulator, the modulator stops powertrain switching and the output voltage of the unit falls. Once the case temperature rises above $T_{CASE\text{-}UTP}$, after a time greater than or equal to t_{OFF}, the unit recovers and undergoes a normal restart.

Output Overvoltage Protection (OVP)

The microcontroller monitors the primary sensed output voltage (as shown on page 6) to detect output OVP. If the primary sensed output voltage exceeds $V_{OUT\text{-}OVLO+}$, a fault is latched, the logic disables the modulator, the modulator stops powertrain switching, and the output voltage of the module falls after a time t_{SOVP}. Faults shorter than a time t_{SOVP} may not be detected. This type of fault is a latched fault and requires that 1) the EN pin be toggled or 2) the input power be recycled to recover from the fault.

Hold-up Capacitance

The VI BRICK AC Front End uses secondary-side energy storage (at the SELV 48 V bus) and optional PRM® regulators to maintain output hold up through line dropouts and brownouts. The module's output bulk capacitance can be sized to achieve the required hold up functionality.

Hold-up time depends upon the output power drawn from the VI BRICK AC Front End based AC-to-DC front end and the input voltage range of downstream DC-to-DC converters.

The following formula can be used to calculate hold-up capacitance for a system comprised of VI BRICK AC Front End and a PRM regulator:

$$C = 2*P_{OUT}*(0.005+t_d)/(V_2^{\,2} - V_1^{\,2})$$

where:

C	VI BRICK AC Front End's output bulk capacitance in farads
t_d	Hold-up time in seconds
P_{OUT}	VI BRICK AC Front End's output power in watts
V_2	Output voltage of VI BRICK AC Front End's converter in volts
V_1	PRM™ regulator undervoltage turn off (volts)
	–OR–
	$P_{OUT}/I_{OUT\text{-}PK}$, whichever is greater.

Output Filtering

The VI BRICK AC Front End module requires an output bulk capacitor in the range of 6,000 µF to 12,000 µF for proper operation of the PFC front-end.

The output voltage has the following two components of voltage ripple:

1) Line frequency voltage ripple: $2*f_{LINE}$ Hz component

2) Switching frequency voltage ripple: 1 MHz module switching frequency component

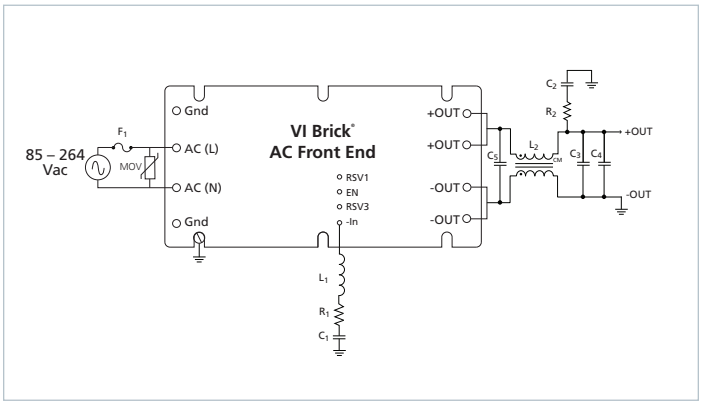


Figure 28 – *Typical Application for EN55022 Class B EMI*

Where, in the schematic:

C_1	2.2nF (Murata GA355DR7GF222KW01L)
C_2	4.7nF (Murata GA355DR7GF472KW01L)
C_3	3.3µF (TDK C4532X7R1H335MT)
C_4	6800uF 63V (Panasonic UVR1J682MRD)
C_5	100uF 63V (Nichicon UVY1J101MPD)
F_1	5A, 216 Series Littlefuse
L_1	15µH (TDK MLF2012C150KT)
L_2	600µH (Vicor 37052-601)
MOV	300V, 10KA, 20mm dia (Littlefuse TMOV20RP300E)
R_1	6.8Ω
R_2	2.2Ω

Line Frequency Filtering

Output line frequency ripple depends upon output bulk capacitance. Output bulk capacitor values should be calculated based on line frequency voltage ripple. High-grade electrolytic capacitors with adequate ripple current ratings, low ESR and a minimum voltage rating of 63 V are recommended.

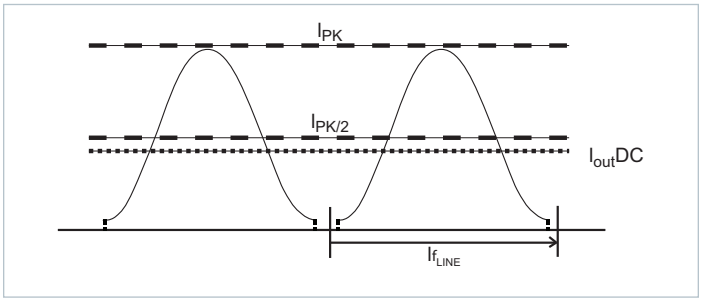


Figure 29 – *Output current waveform*

Product Details and Design Guidelines (cont.)

Based on the output current waveform, as seen in Figure 29, the following formula can be used to determine peak-to-peak line frequency output voltage ripple:

$$V_{PP}l \cong 0.2 * P_{OUT}/(V_{OUT} * f_{LINE} * C)$$

where:

$V_{PP}l$	Output voltage ripple Peak-to-peak line frequency
P_{OUT}	Average output power
V_{OUT}	Output voltage set point, nominally 48 V
f_{LINE}	Frequency of line voltage
C	Output bulk capacitance
I_{DC}	Maximum average output current
I_{PK}	Peak-to-peak line frequency output current ripple

In certain applications, the choice of bulk capacitance may be determined by hold-up requirements and low frequency output voltage filtering requirements. Such applications may use the greater capacitance value determined from these requirements. The ripple current rating for the bulk capacitors can be determined from the following equation:

$$I_{ripple} \cong 0.8 * P_{OUT}/V_{OUT}$$

Switching Frequency Filtering

Some applications require the output filtering shown in figure 28 to meet radiated emissions limits. In such a situation, the output switching ripple shown in figure 6 should be expected at the output of the filter. In cases where other means are used to control radiated emissions, and more ripple can be tolerated, the output filter can be simplified by removal of the common mode inductor, and C5, which is used to reduce the Q of the LC resonant tank.

Output switching frequency voltage ripple is the function of the output bypass ceramic capacitor. Output bypass ceramic capacitor values should be calculated based on switching frequency voltage ripple. Normally bypass capacitors with low ESR are used with a sufficient voltage rating.

Output bypass ceramic capacitor value for allowable peak-to-peak switching frequency voltage ripple can be determined by:

$$C_3 = Q_{TOT} / V_{OUT\text{-}PP\text{-}HF} - C_{OUT\text{-}INT}$$

where:

$V_{OUT\text{-}PP\text{-}HF}$	Allowable peak-to-peak output switching frequency voltage ripple in volts
Q_{TOT}	The total output charge per switching cycle at full load, maximum 13.5 µC
C_{OUT_INT}	The module internal effective capacitance
C_3	Required output bypass ceramic capacitor

EMI Filtering and Transient Voltage Suppression

EMI Filtering

The VI BRICK AC® Front End with PFC is designed such that it will comply with EN55022 Class B for Conducted Emissions with the filter connected across -IN and GND as shown in Figure 28. The emissions spectrum is shown in Figures 13-16. If one of the outputs is connected to earth ground, a small (single turn) output common mode choke is also required.
EMI performance is subject to a wide variety of external influences such as PCB construction, circuit layout etc. As such, external components in addition to those listed herein may be required in specific instances to gain full compliance to the standards specified.

Transient Voltage Suppression

The VI Brick AC Front End contains line transient suppression circuitry to meet specifications for surge (i.e. EN61000-4-5) and fast transient conditions (i.e. EN61000-4-4 fast transient/"burst").

Thermal Design

Thermal management of internally dissipated heat should maximize heat removed from the baseplate surface, since the baseplate represents the lowest aggregate thermal impedance to internal components. The baseplate temperature should be maintained below 100°C. Cooling of the system PCB should be provided to keep the leads below 100°C, and to control maximum PCB temperatures in the area of the module.

Powering a Constant Power Load

When the output voltage of the VI BRICK AC Front End module is applied to the input of the PRM® regulator, the regulator turns on and acts as a constant-power load. When the module's output voltage reaches the input undervoltage turn on of the regulator, the regulator will attempt to start. However, the current demand of the PRM® regulator at the undervoltage turn-on point and the hold-up capacitor charging current may force the VI BRICK AC Front End into current limit. In this case, the unit may shut down and restart repeatedly. In order to prevent this multiple restart scenario, it is necessary to delay enabling a constant-power load when powered up by the upstream AC to 48 V front end until after the output set point of the VI BRICK AC Front End is reached.

This can be achieved by

1) keeping the downstream constant-power load off during power up sequence

   and

2) turning the downstream constant-power load on after the output voltage of the module reaches 48 V steady state.

After the initial startup, the output of the VI BRICK AC Front End can be allowed to fall to 30 V during a line dropout at full load. In this case, the circuit should not disable the PRM regulator if the input voltage falls after it is turned on; therefore, some form of hysteresis or latching is needed on the enable signal for the constant power load. The output capacitance of the VI BRICK AC Front End should also be sized appropriately for a constant power load to prevent collapse of the output voltage of the module during line dropout (see Hold up Capacitance on page 17). A constant-power load can be turned off after completion of the required hold up time during the power-down sequence or can be allowed to turn off when it reaches its own undervoltage shutdown point.

Product Details and Design Guidelines (cont.)

The timing diagram in Figure 30 shows the output voltage of the VI BRICK® AC Front End module and the PRM® PC pin voltage and output voltage of the PRM regulator for the power up and power down sequence. It is recommended to keep the time delay approximately 10 to 20 ms.

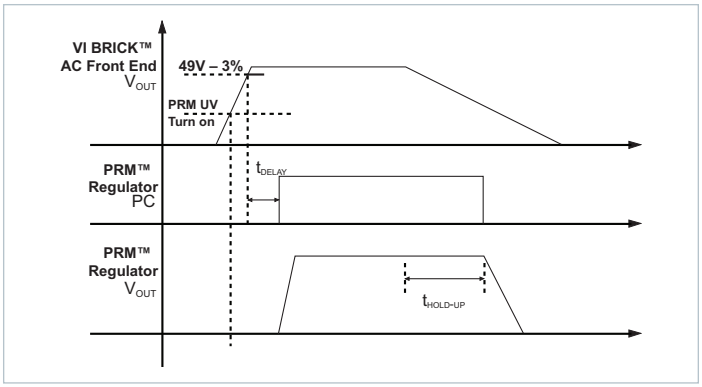


Figure 30 – *PRM Enable Hold off Waveforms*

Special care should be taken when enabling the constant-power load near the auto-ranger threshold, especially with an inductive source upstream of the VI BRICK AC Front End. A load current spike may cause a large input voltage transient, resulting in a range change which could temporarily reduce the available power (see Adaptive Cell™ Topology below).

Adaptive Cell™ Topology

The Adaptive Cell topology utilizes magnetically coupled "top" and "bottom" primary cells that are adaptively configured in series or parallel by a configuration controller comprised of an array of switches. A microcontroller monitors operating conditions and defines the configuration of the top and bottom cells through a range control signal.

A comparator inside the microcontroller monitors the line voltage and compares it to an internal voltage reference.
If the input voltage of the VI BRICK AC Front End crosses above the positive going cell reconfiguration threshold voltage, the output of the comparator transitions, causing switches S_1 and S_2 to open and switch S_3 to close (see Functional Block Diagram on page 6). With the top cell and bottom cell configured in series, the unit operates in "high" range and input capacitances C_{IN-T} and C_{IN-B} are in series.

If the peak of input voltage of the unit falls below the negative-going range threshold voltage for two line cycles, the cell configuration controller opens switch S_3 and closes switches S_1 and S_2. With the top cell and bottom cells configured in parallel, the unit operates in "low" range and input capacitances C_{IN-T} and C_{IN-B} are in parallel.

Power processing is held off while transitioning between ranges and the output voltage of the unit may temporarily droop. External output hold up capacitance should be sized to support power delivery to the load during cell reconfiguration. The minimum specified external output capacitance of 6,000 µF is sufficient to provide adequate ride-through during cell reconfiguration for typical applications.

Vicor's comprehensive line of power solutions includes high density AC-DC and DC-DC modules and accessory components, fully configurable AC-DC and DC-DC power supplies, and complete custom power systems.

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